Kandou's Chordal Coding for Chip-to-Chip Communication

Amin Shokrollahi

KANDOU BUS

In collaboration with
the Kandou Bus team

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ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

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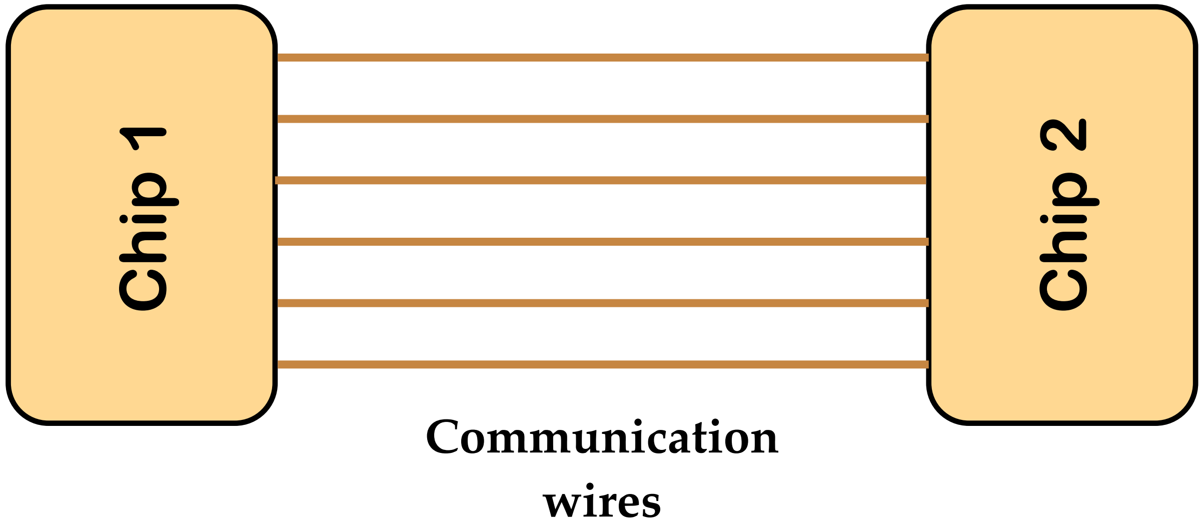
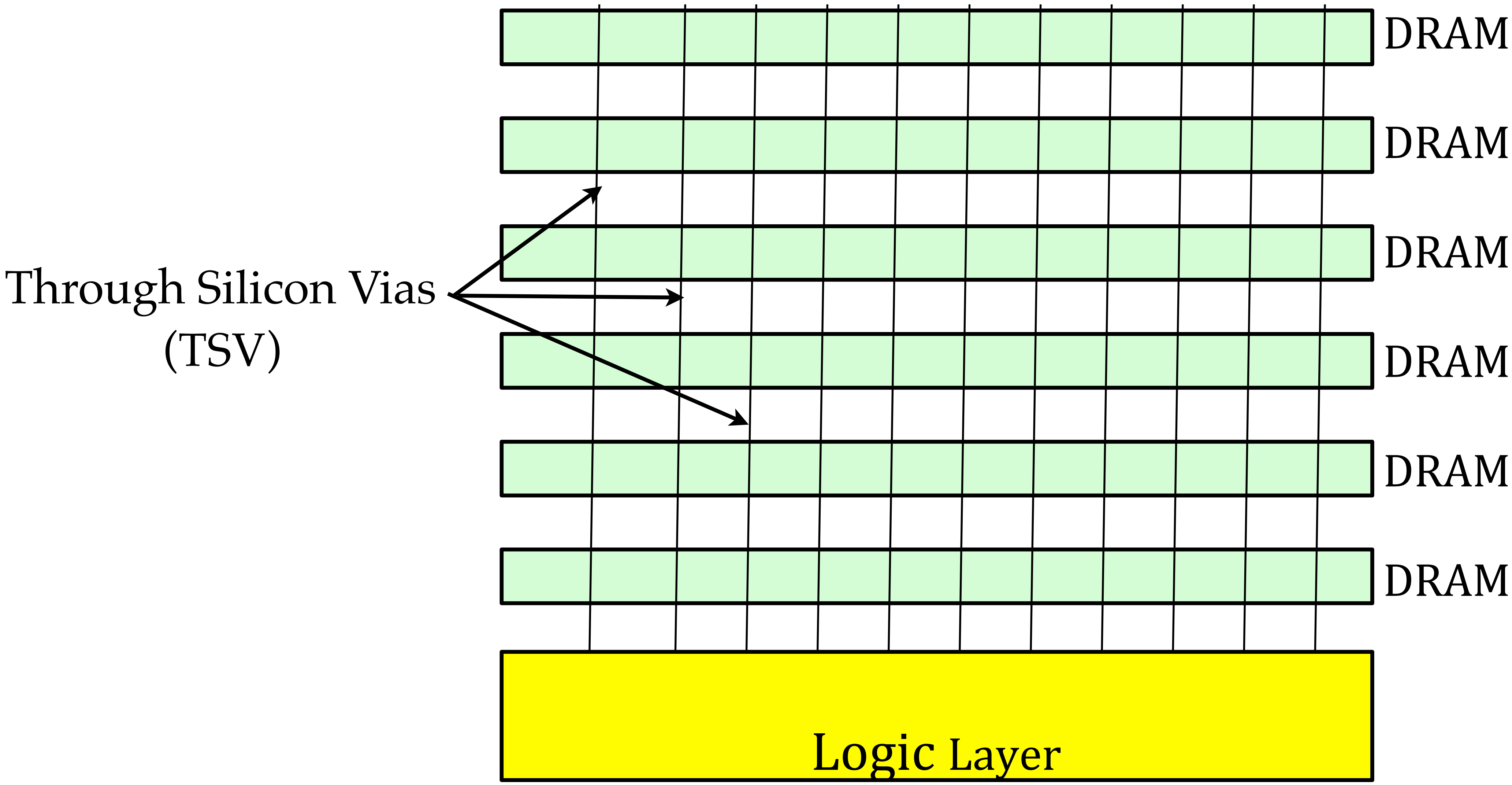
Chip-to-Chip Communication



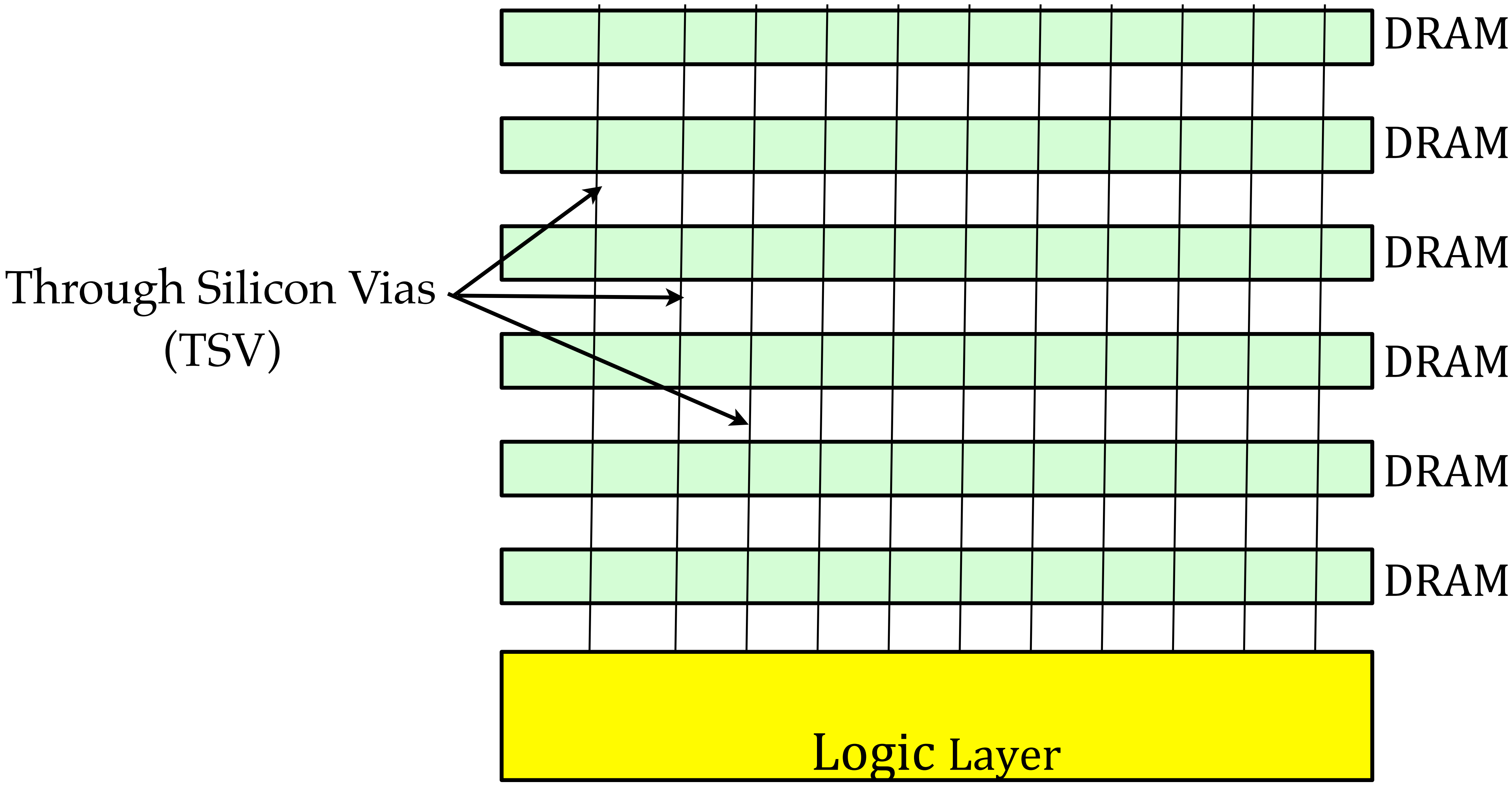
Task: reliably transmit information from Chip 1 to Chip 2

Examples



DRAM
DRAM
DRAM
DRAM
DRAM
DRAM
Through Silicon Vias
(TSV)
Logic Layer

Examples



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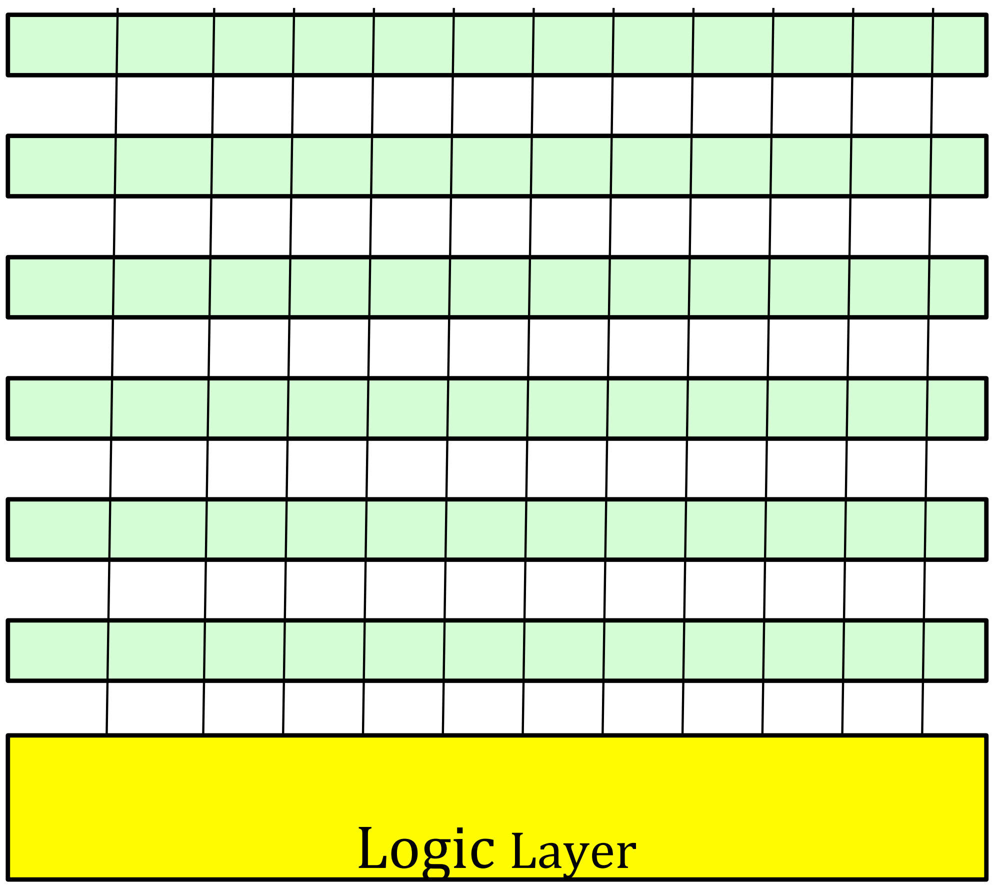
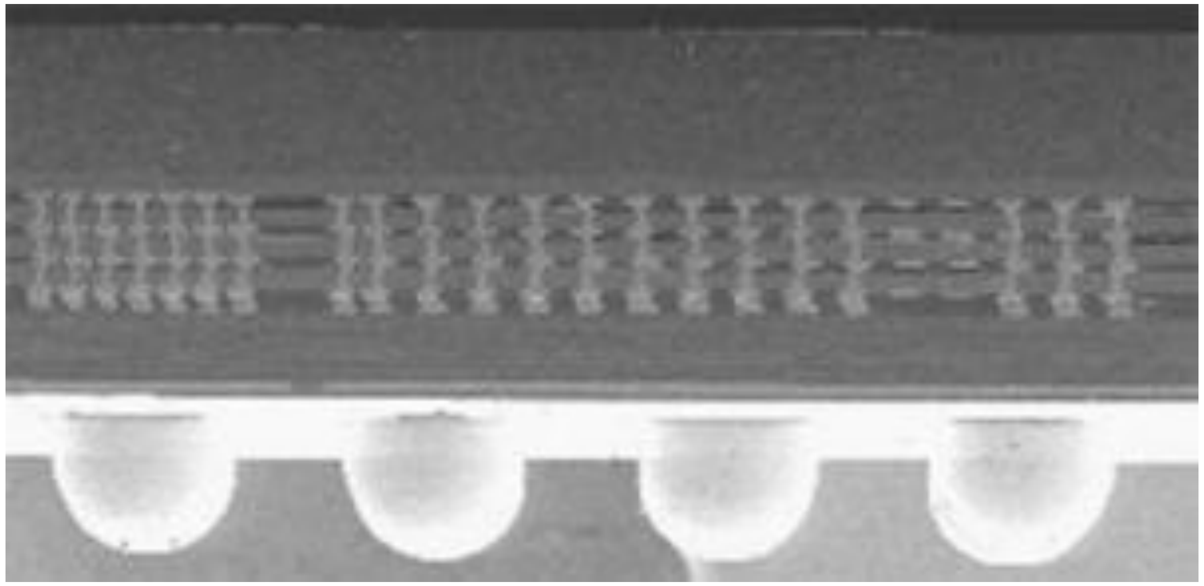
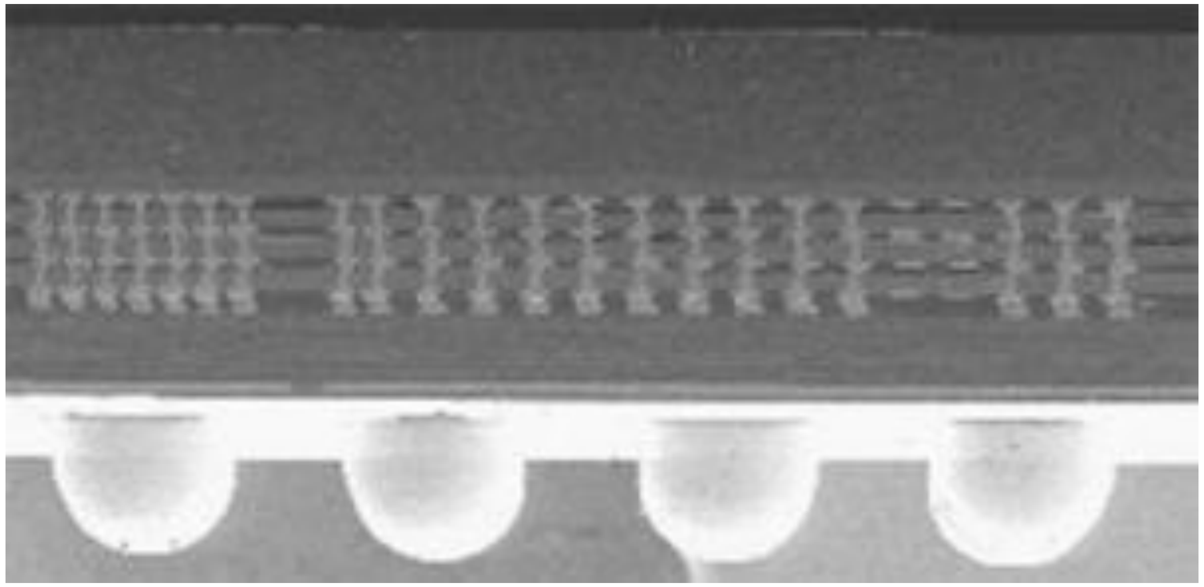




DRAM stacking with TSV
Communication between DRAM and base layer

Examples



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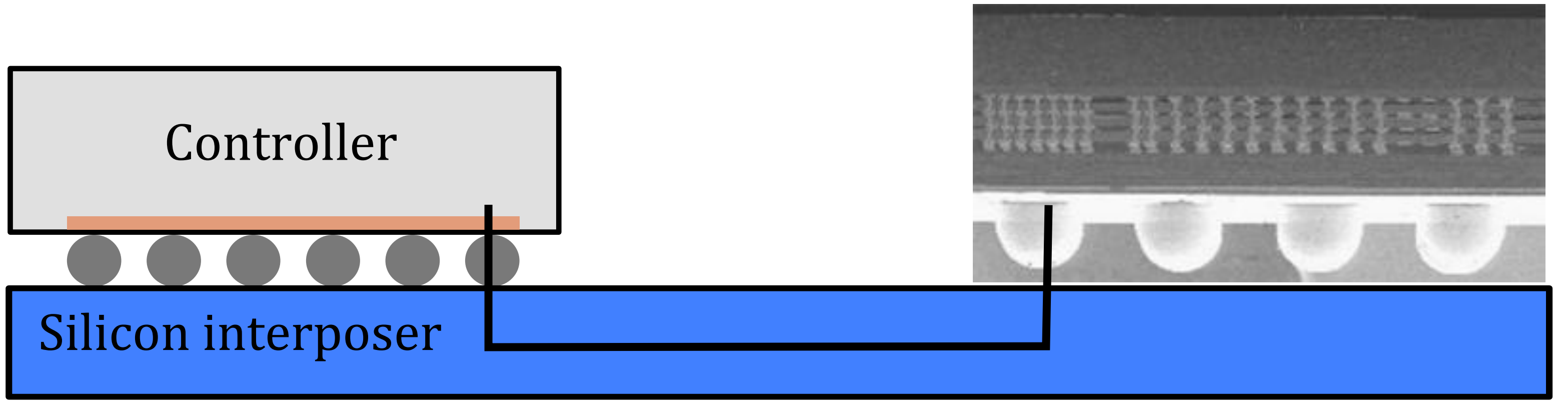
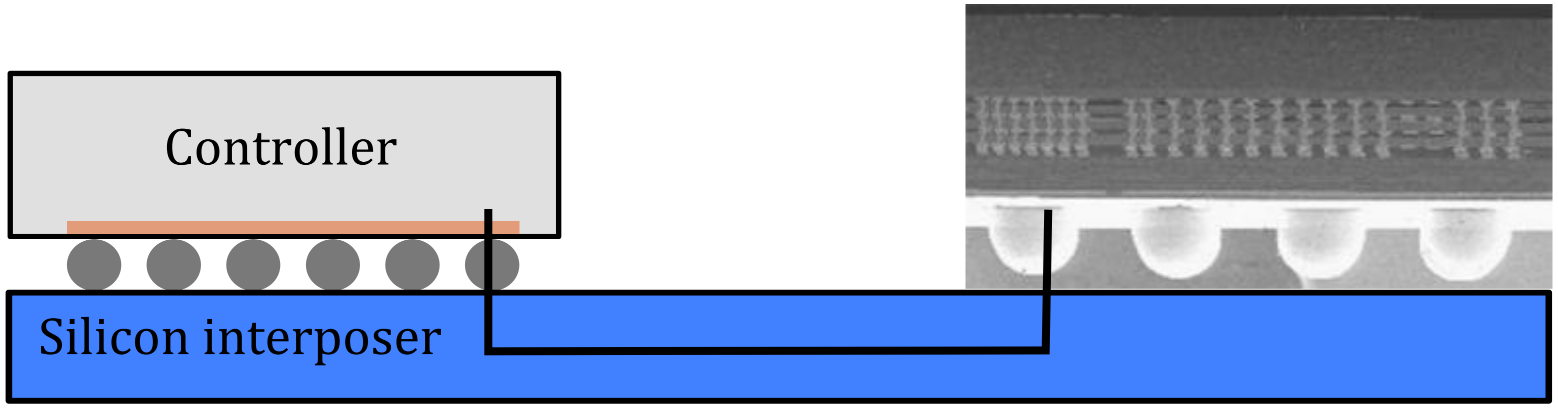


Examples



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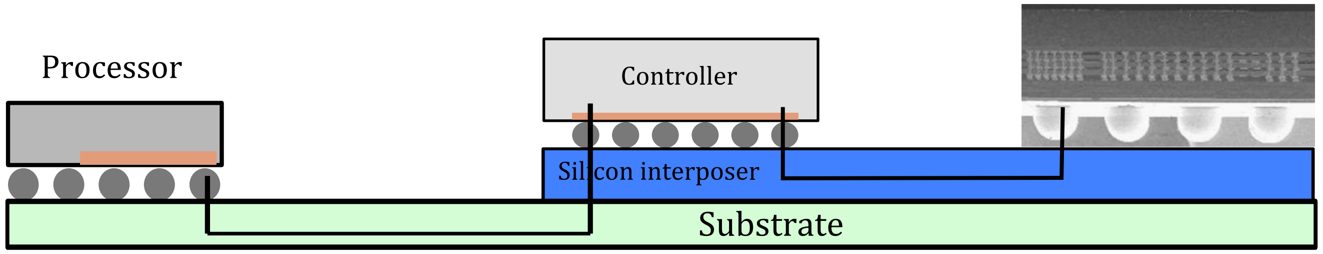
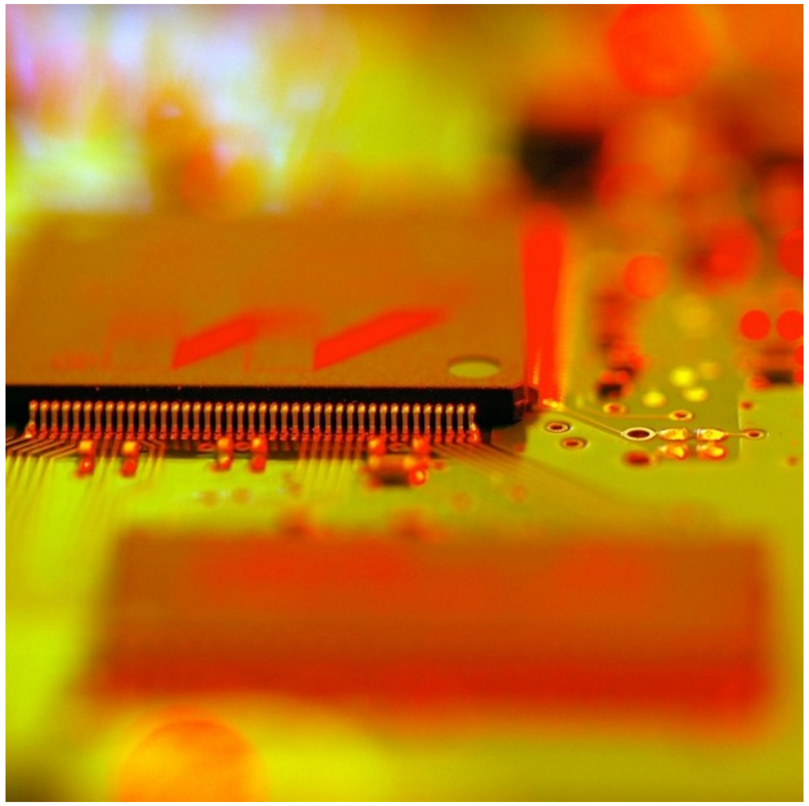


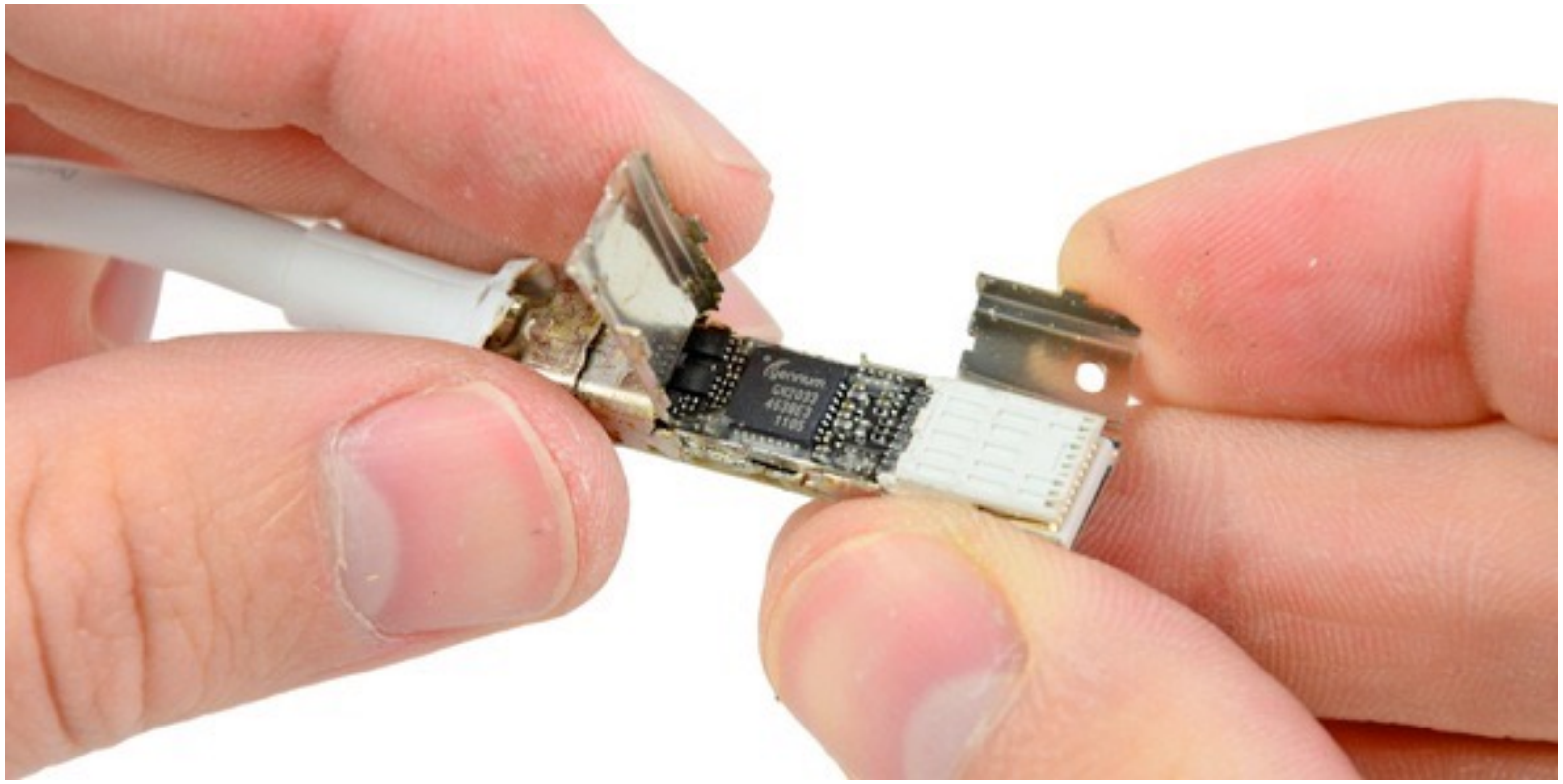
Communication with processor
Controller could be connected to ADC
ADC to optical interface (Tbps comm)
Processor could be connected to 400GE link

Examples



Memory - processor interface
DDRx, GDDRx, LPDDRx

Examples



Device-to-device connection via active cables (Picture: Thunderbolt)

In Short….

- Abundant applications (networking, mobile devices, displays, automotive,…..)
- Connection speeds are increasing, real estate is shrinking
- Need to transmit more bits per second on every wire.

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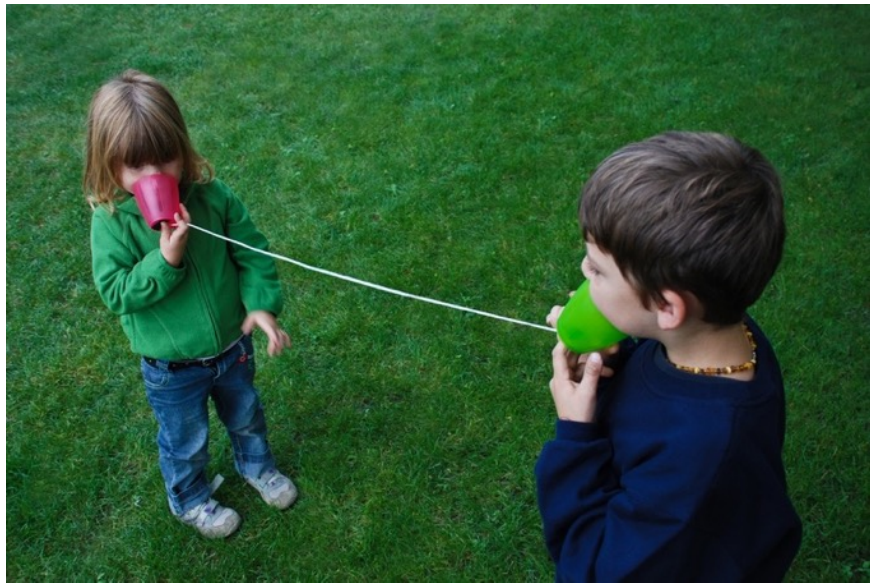
Communication Channel



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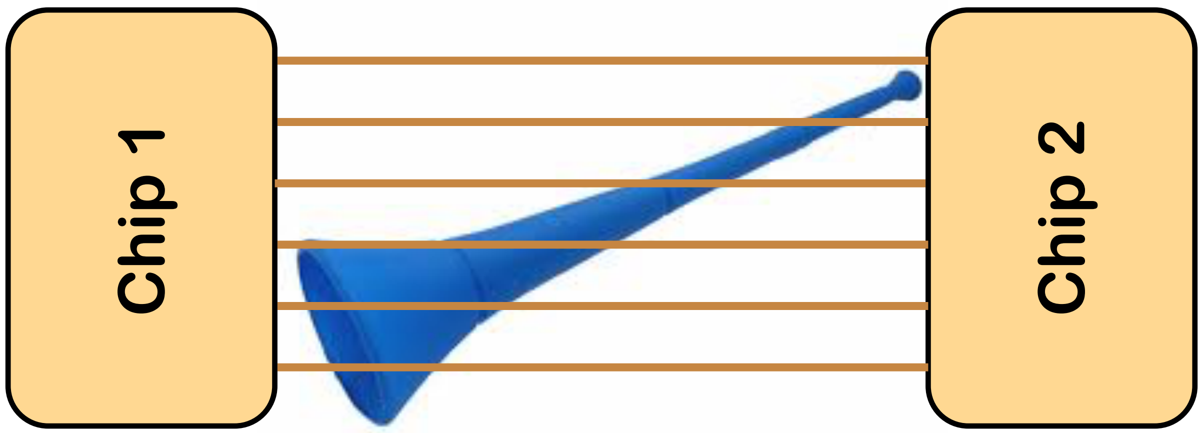
Noise

Noise



What it is not

Or any channel with a lot of "random" noise

Recovery Process

Extremely limited on resources

Rule of 1000's

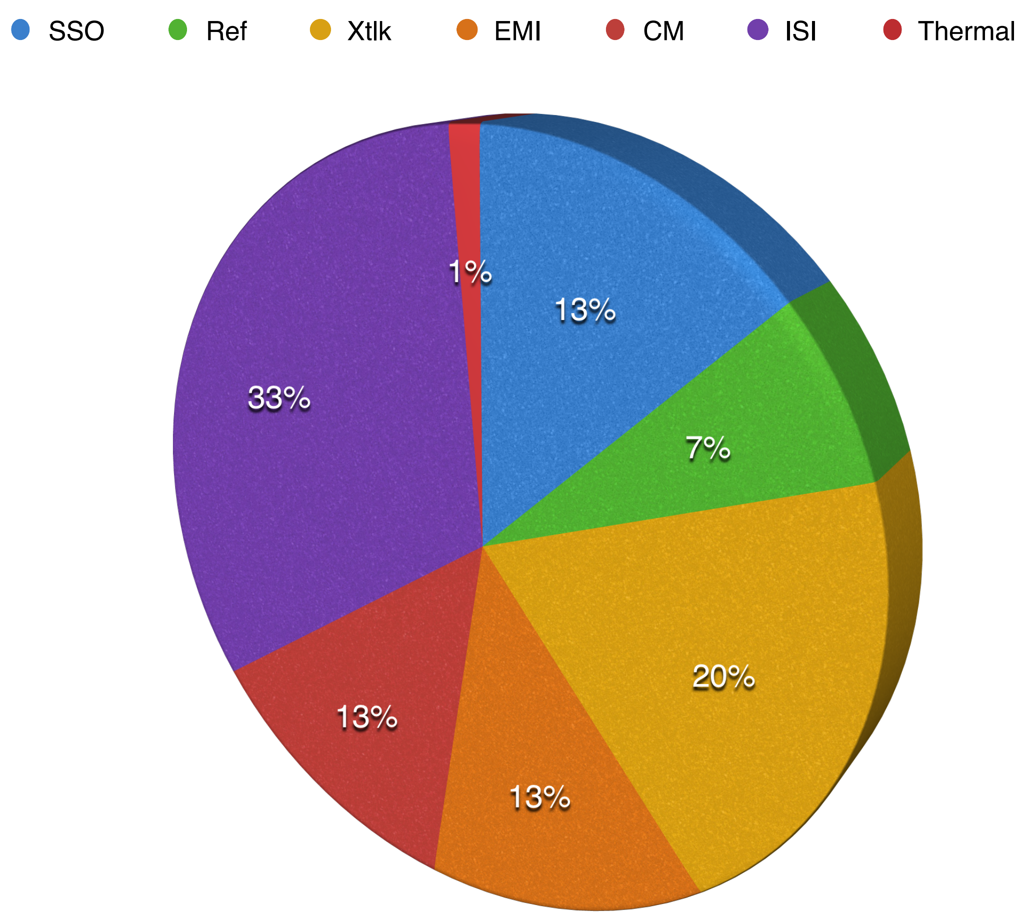
	Throughput	Energy/bit	Recovery time/ bit
Wireless	Mbps	nJ	nano-second
Chip-to-Chip	Gbps	pJ	pico-second

Hardly any power or time to recover a transmitted bit

Noise Types

- Simultaneous Switching Output (SSO) noise
  - Caused by changing current draws from symbol to symbol.
- Reference noise
  - Reference voltages may not be the same at transmitter and receiver
- Crosstalk
  - Transition on one wire effects the voltage/current on nearby wires
- Electromagnetic Interference (EMI) noise
  - High frequency currents on a wire make it an antenna (affects other wires, and is affected by them)
- Common Mode (CM) noise
  - Power supply may bounce up and down; voltage levels on wires can go up and down by the same amount.
- Inter-symbol Interference (ISI) noise
  - Symbols "bleed" into subsequent symbols
- Thermal noise
  - Random jitter

Noise Types



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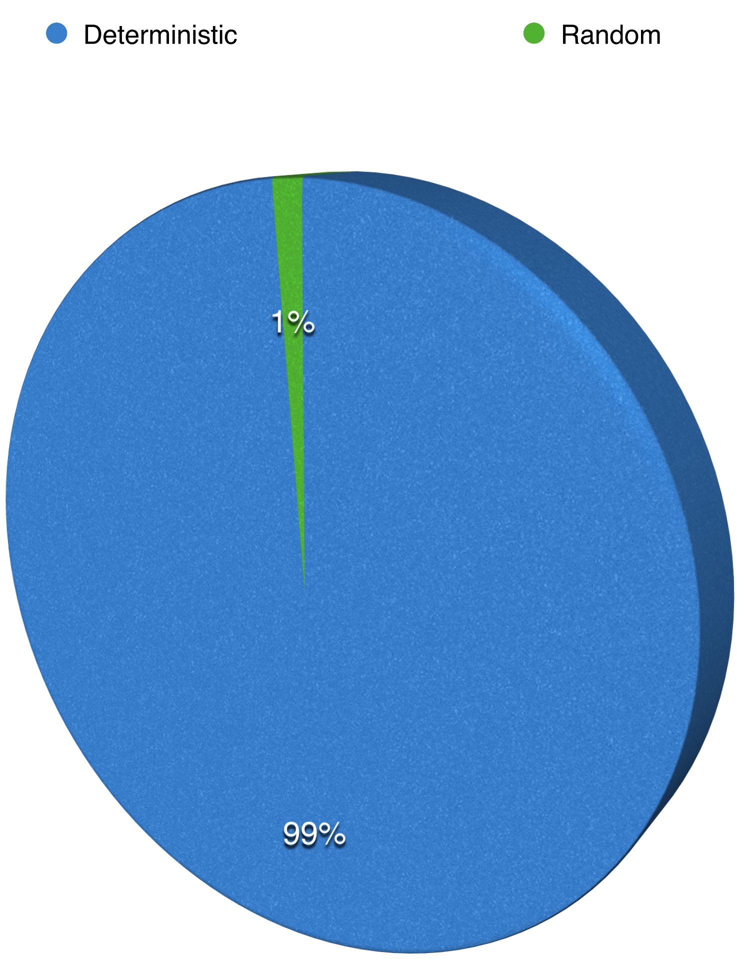
Noise Types



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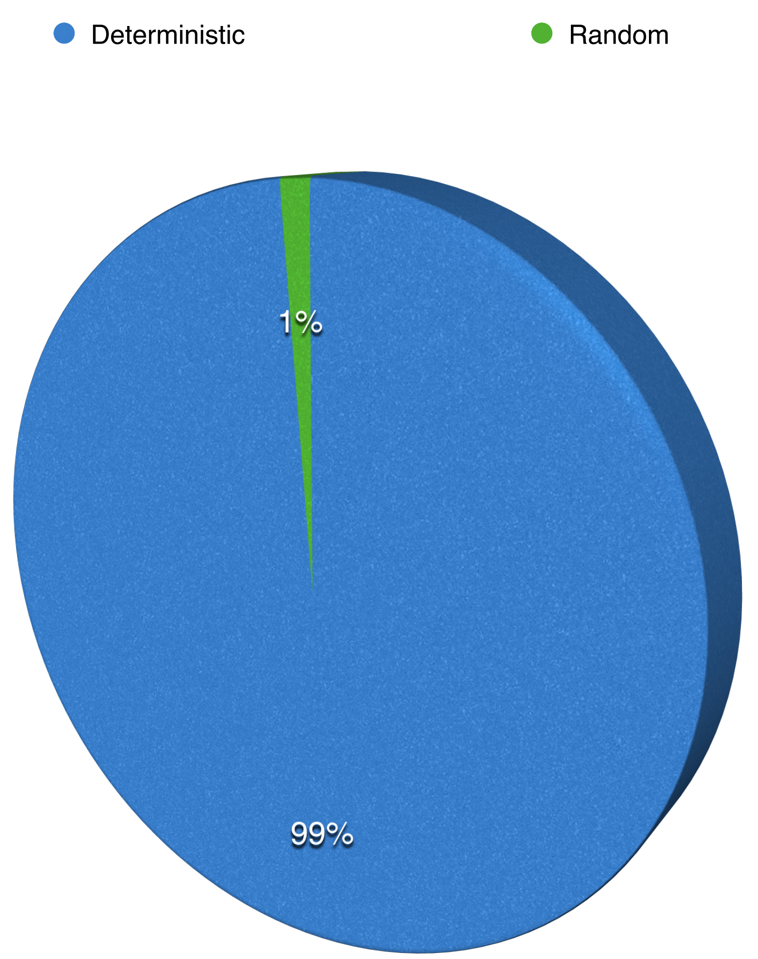

Almost all the noise is deterministic
but resources are tight

Noise Mitigation

	Mitigation techniques
SSO	Modulation, design
Ref	Modulation, design
Xtlk	Layout, design
EMI	Shielding, modulation
Common mode	Modulation, design
ISI	Equalization, modulation
Thermal	Design

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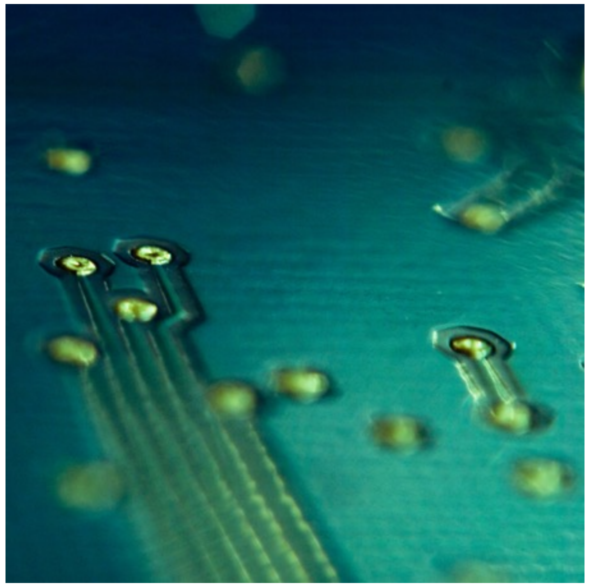
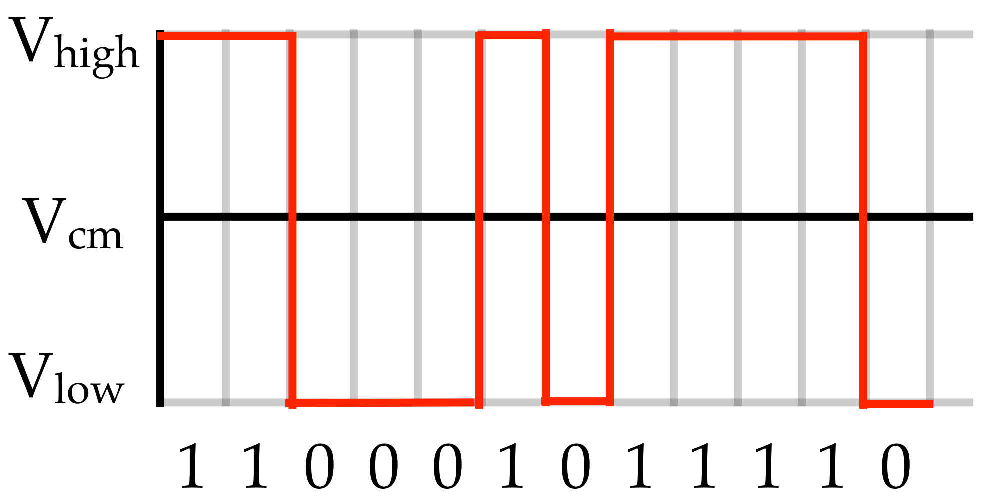
Thermal	Design

Current Modulation Techniques

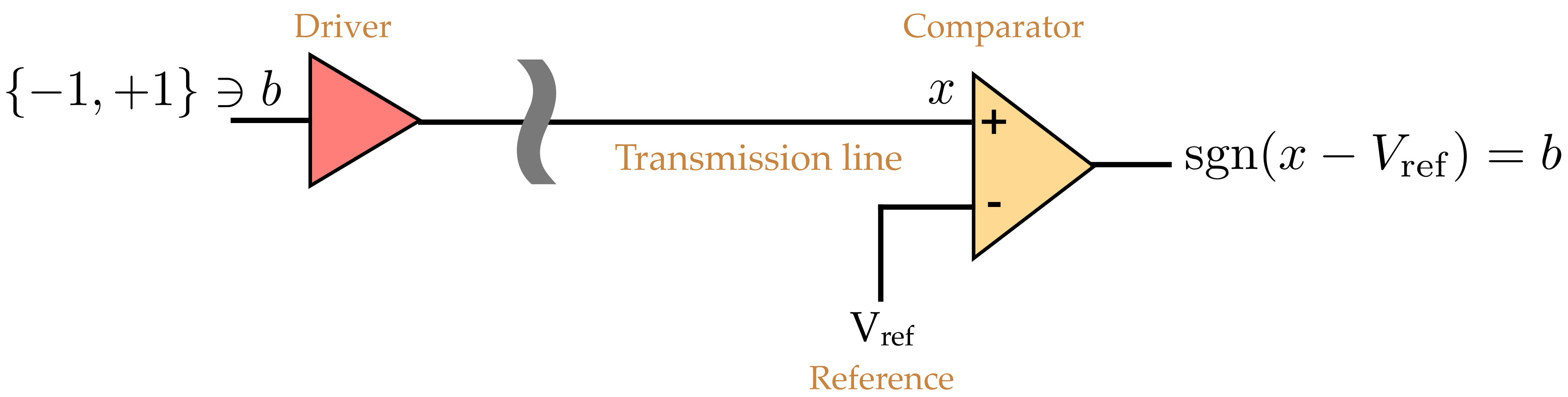


Modulation = Signaling

- Any form of transmitting information through different voltage (current) levels on the communication wires
- Non-Return-to-Zero (NRZ) signaling: good for fast data transmission



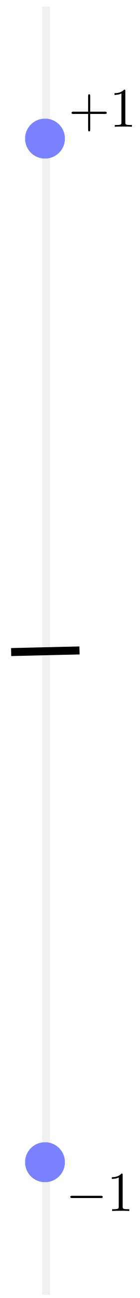
Simple Receiver



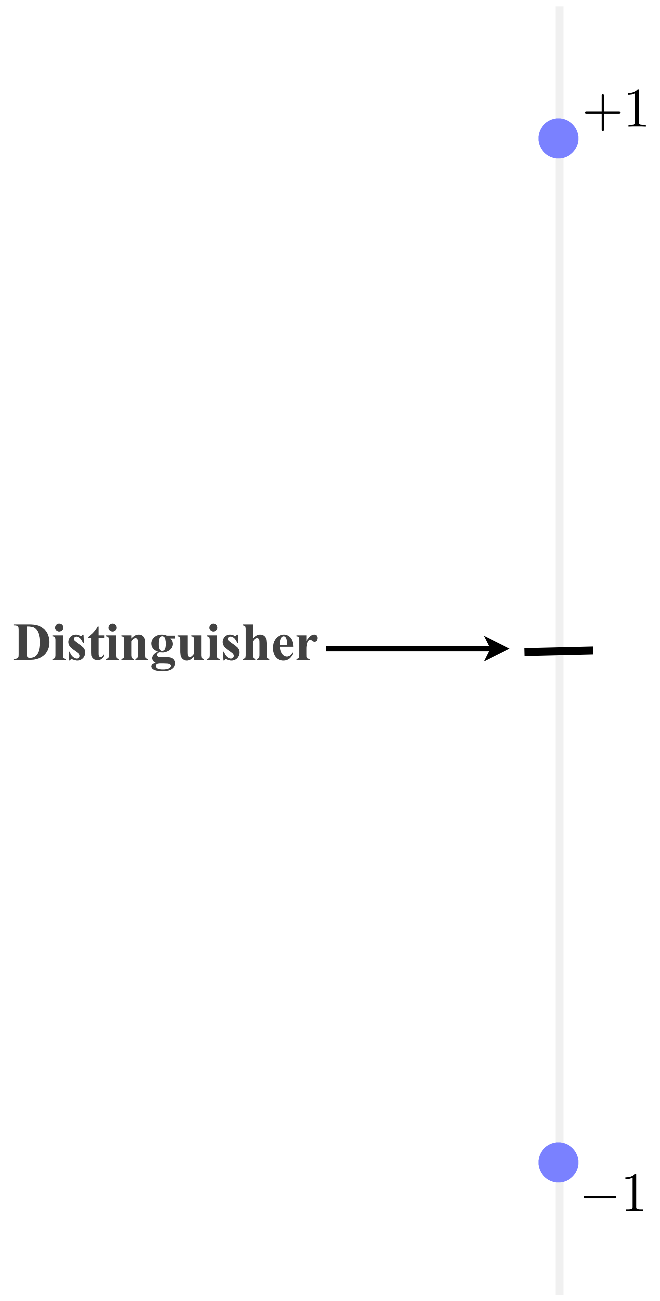
Single-ended Signaling

Transmits one bit per wire

Single Ended Signaling



Single Ended Signaling



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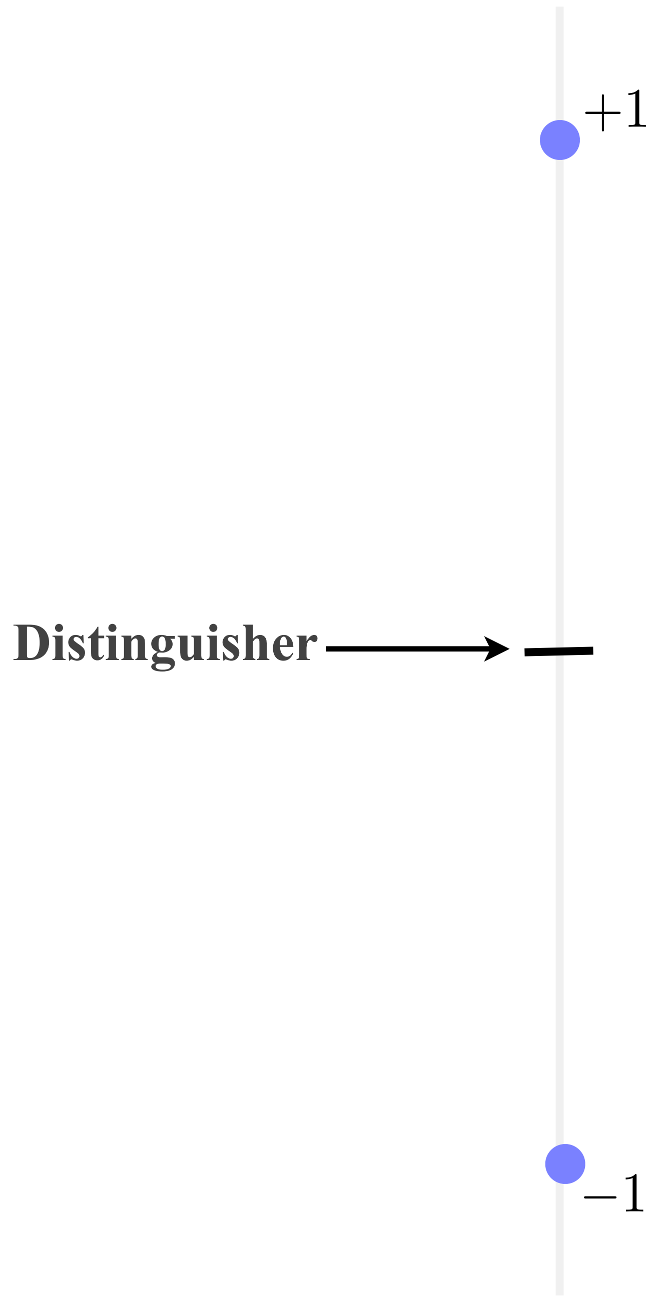

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Noise Immunity

	Single-ended
SSO	-
Ref	-
EMI	-
Common mode	-
ISI	+
Conclusion	Not good for very high speed communication

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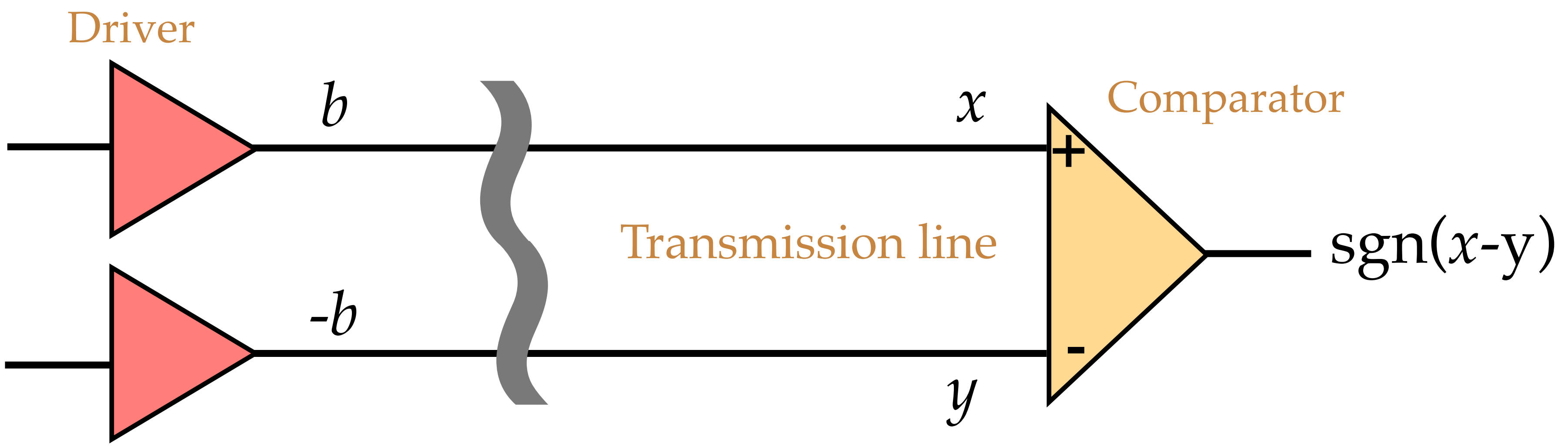
Differential Signaling



Transmits one bit per *a pair* of wires

Noise Immunity

	Single-ended	Differential
SSO	-	+
Ref	-	+
EMI	-	+
Common mode	-	+
ISI	+	-
Conclusion	Not good for very high speed communication	pin count can be a problem

Other Solutions?

- Lower the frequency, i.e., send more data per clock cycle
- How?

Other Solutions?

- Lower the frequency, i.e., send more data per clock cycle

- How?
  - Allow detection of more than 2 states on a single wire, or on two wires
    - ➡ 4-PAM signaling: 4 states, i.e., 2 bits
    - ➡ 8-PAM signaling: 8 states, i.e., 3 bits
    - ➡ What happens to noise?

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	Single-ended	Differential	4-PAM diff.
SSO	-	+	+/-
Ref	-	+	-
EMI	-	+	+
Common mode	-	+	+
ISI	+	-	- -
Conclusion	High speed problematic	Pin count problematic	High speed issues

Other Solutions?

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  - Or, pool more than two wires together
    - ➡ Can this be done?
    - ➡ How much more data can be sent?
    - ➡ What happens to noise?
    - ➡ Etc.

Other Solutions?

- Lower the frequency, i.e., send more data per clock cycle

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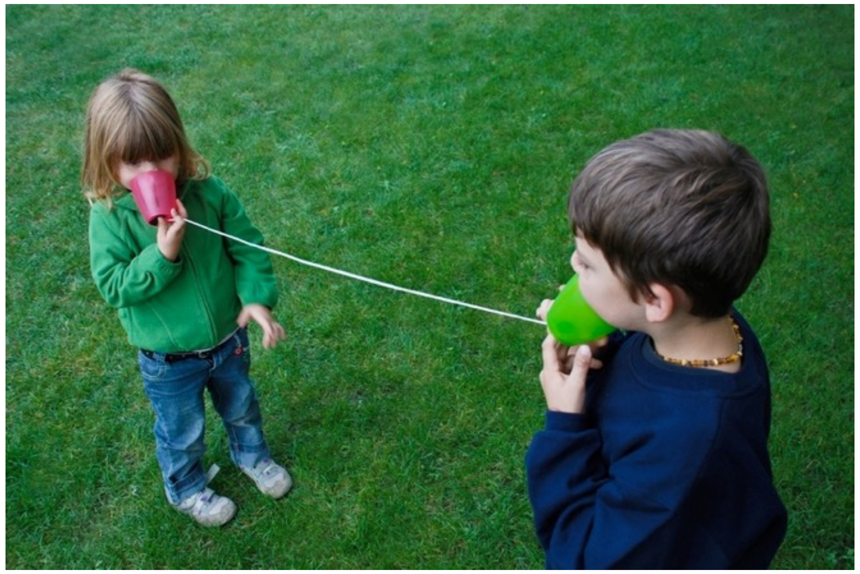
Chord signaling

Theory of Chord Signaling



What I will be Talking about

How to arrive at a new type of coding theory

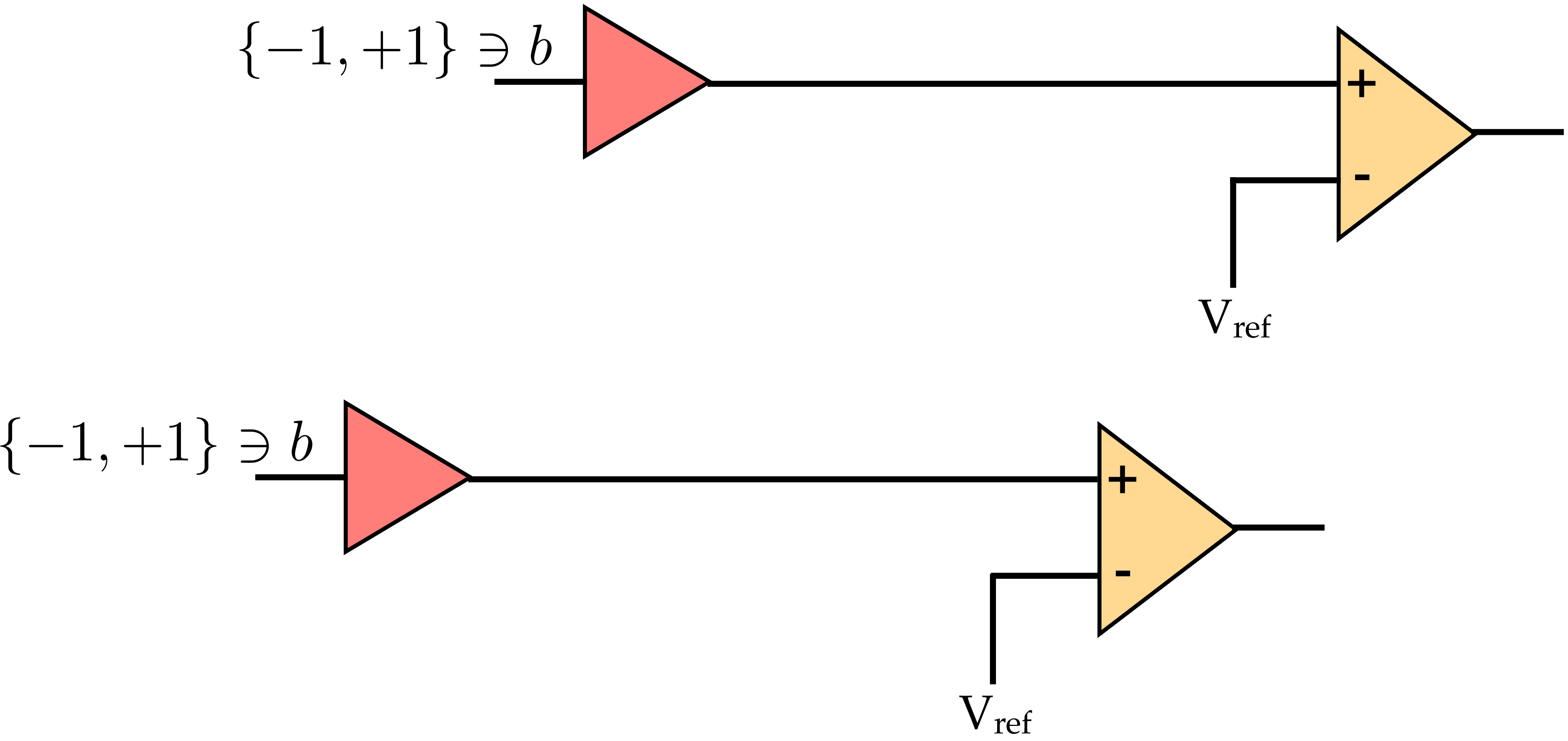
What I will not be Talking about

Constructions, solutions, etc

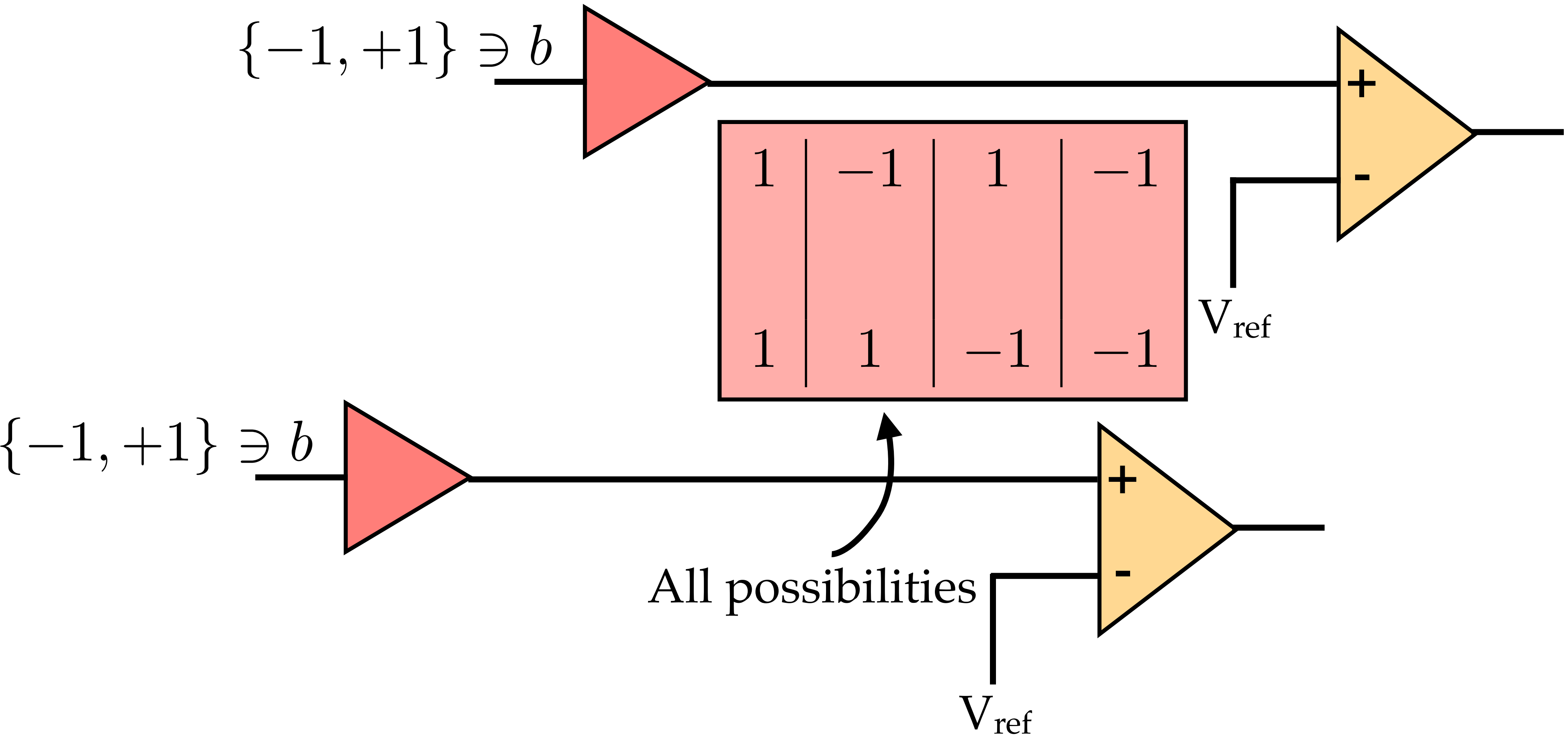
Test chips, electronics behind it, etc

Two Independent Wires

Two Independent Wires



Two Independent Wires

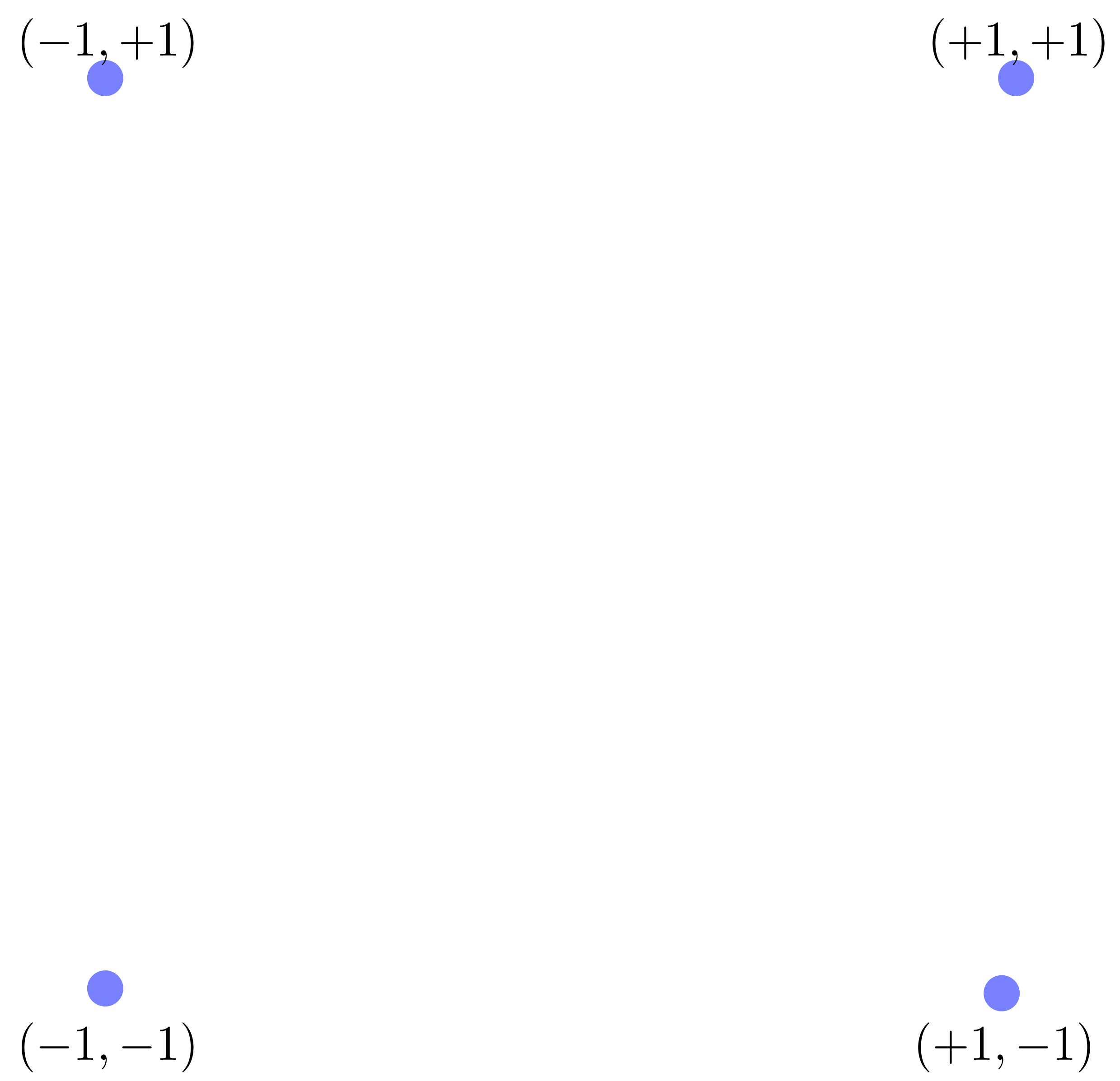


Abstraction

Think of the simultaneous values on the wires as points in the 2-dimensional space

Geometric View

Geometric View



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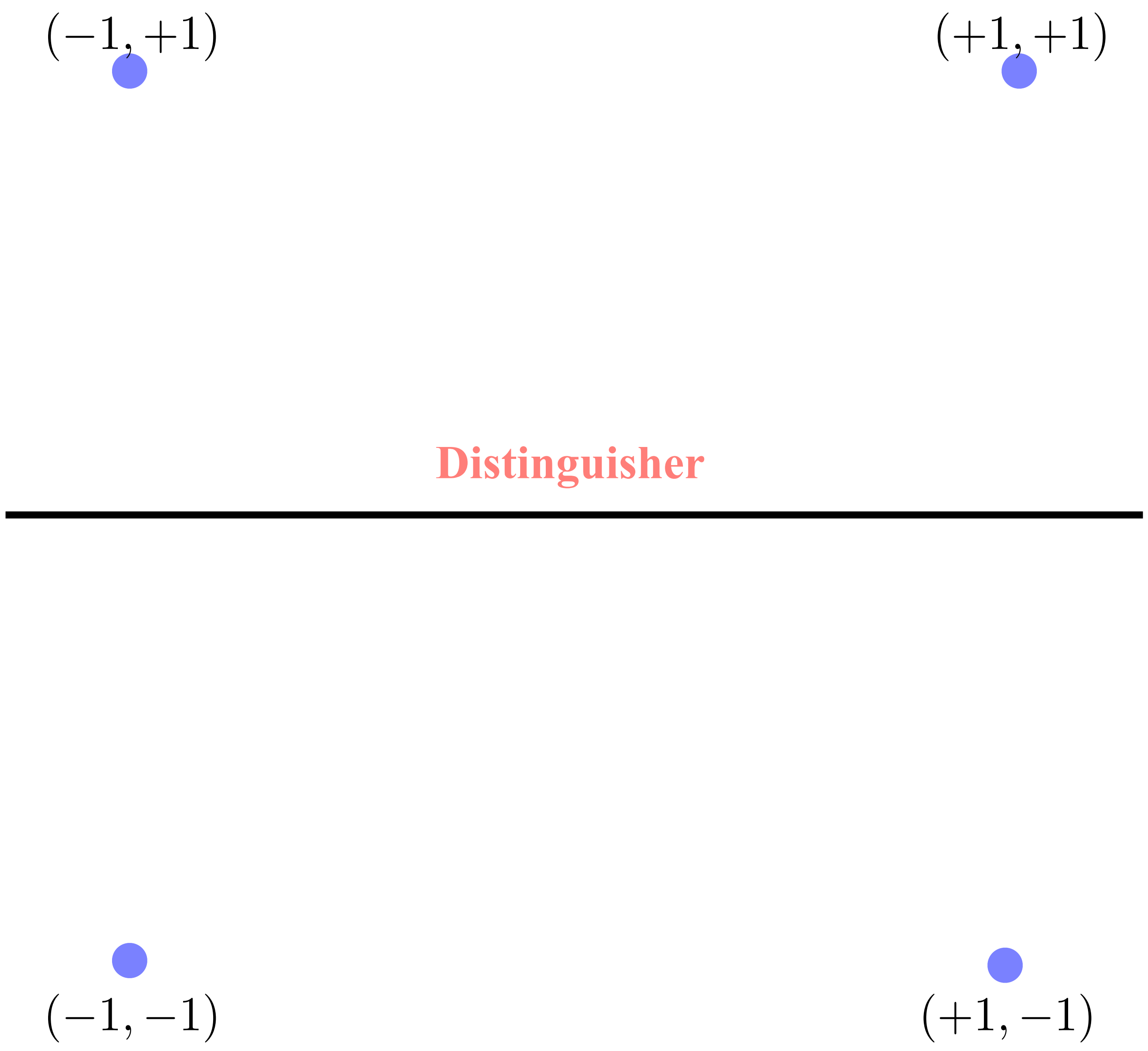

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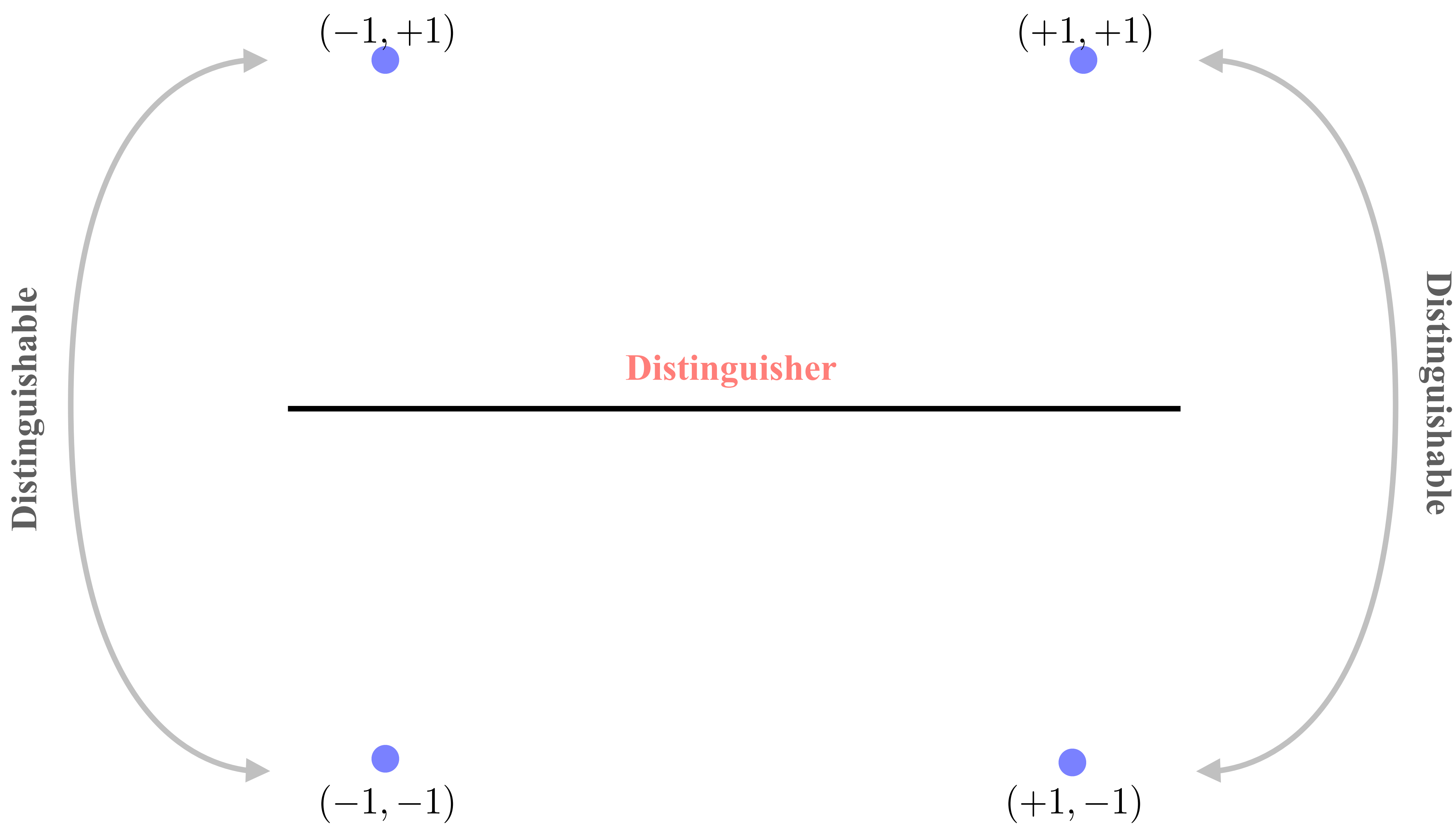

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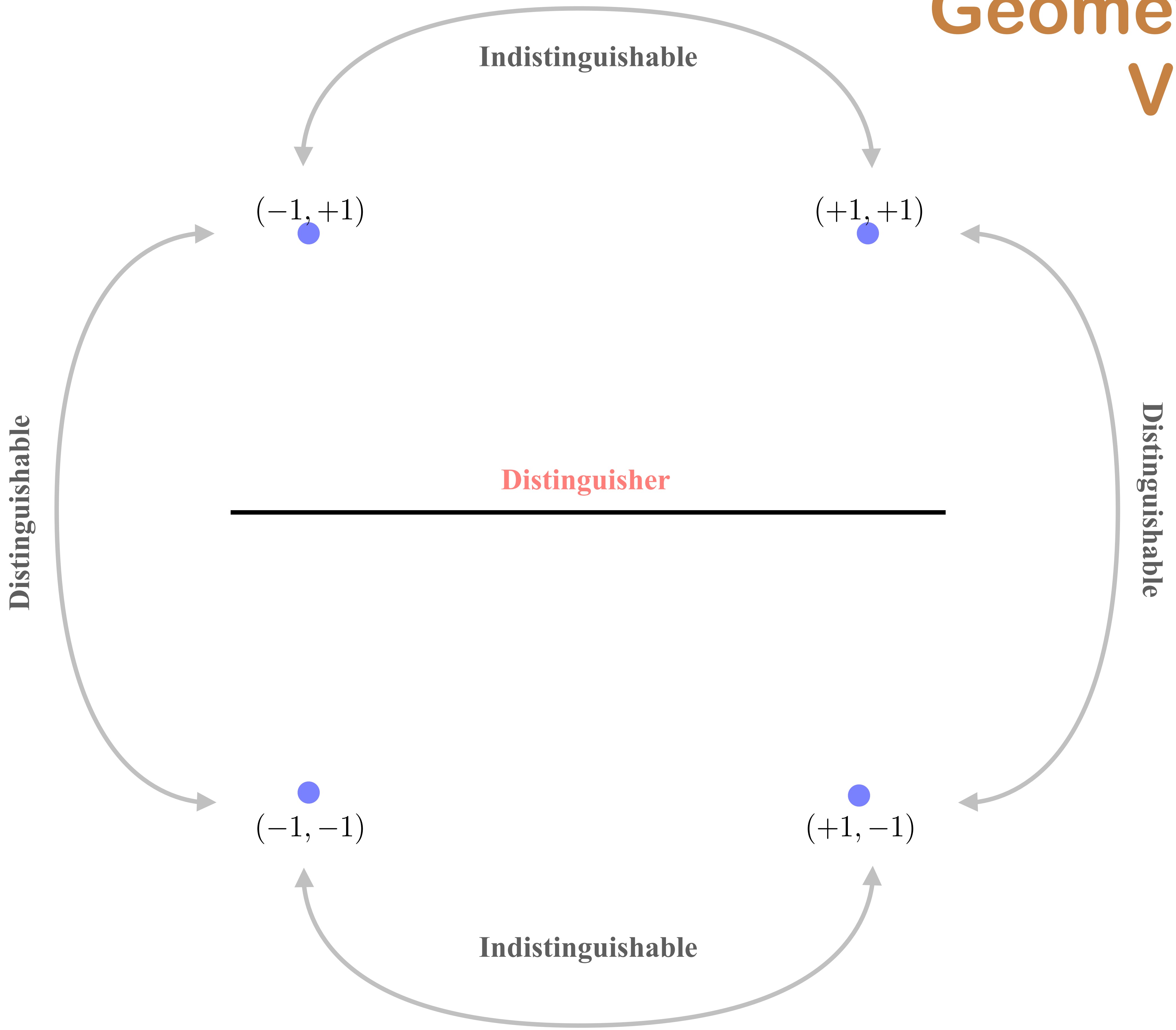

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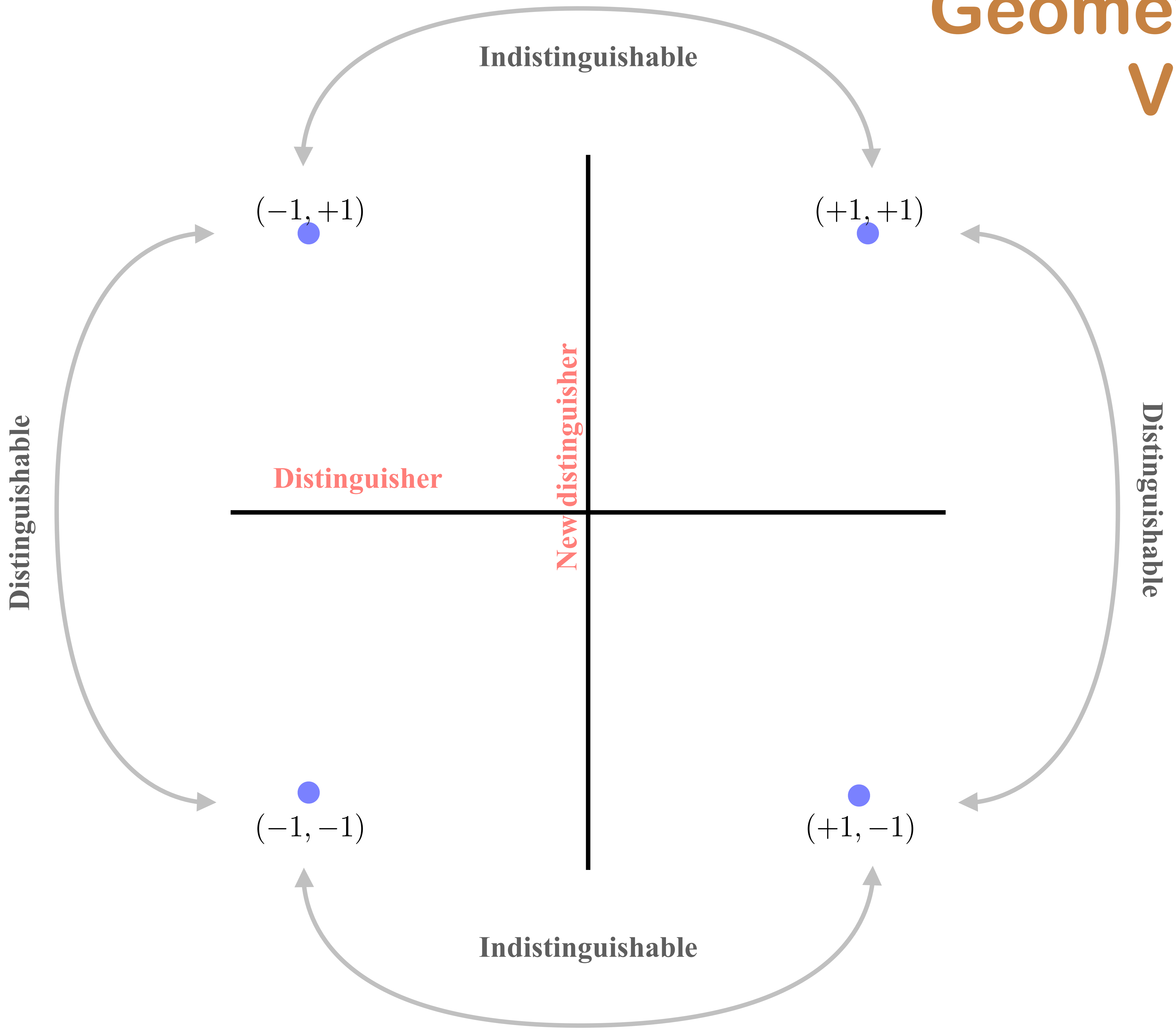

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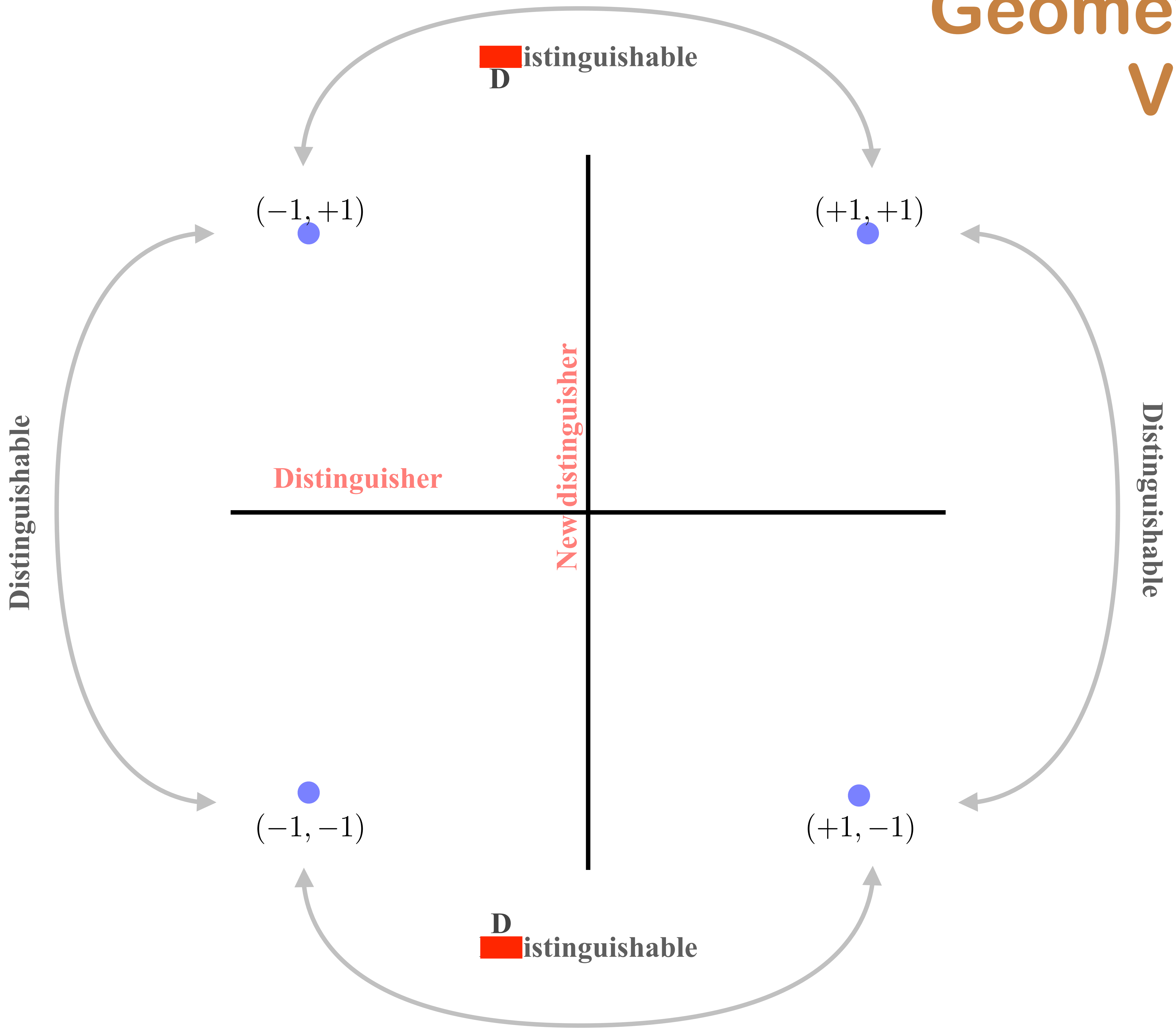

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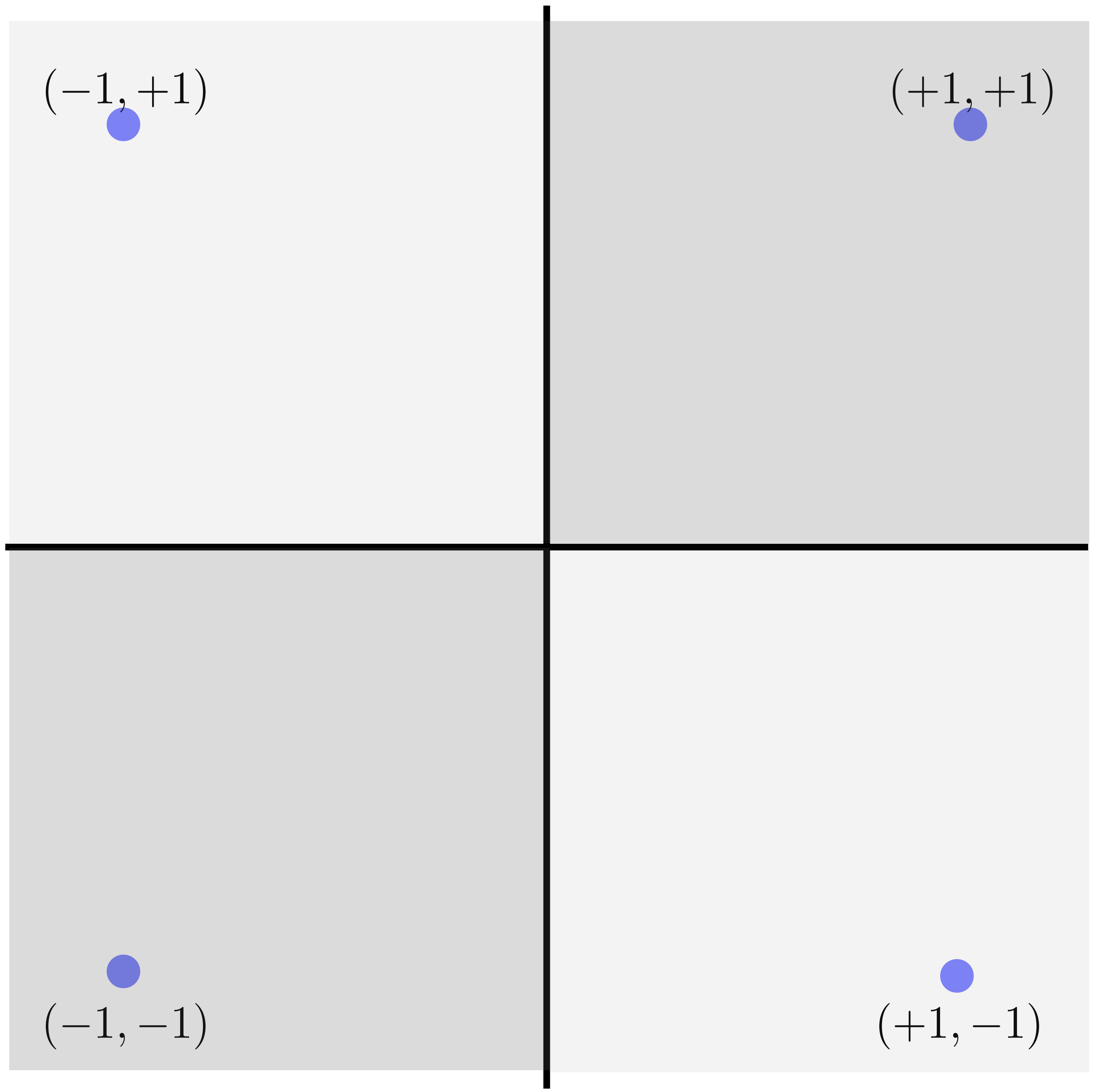


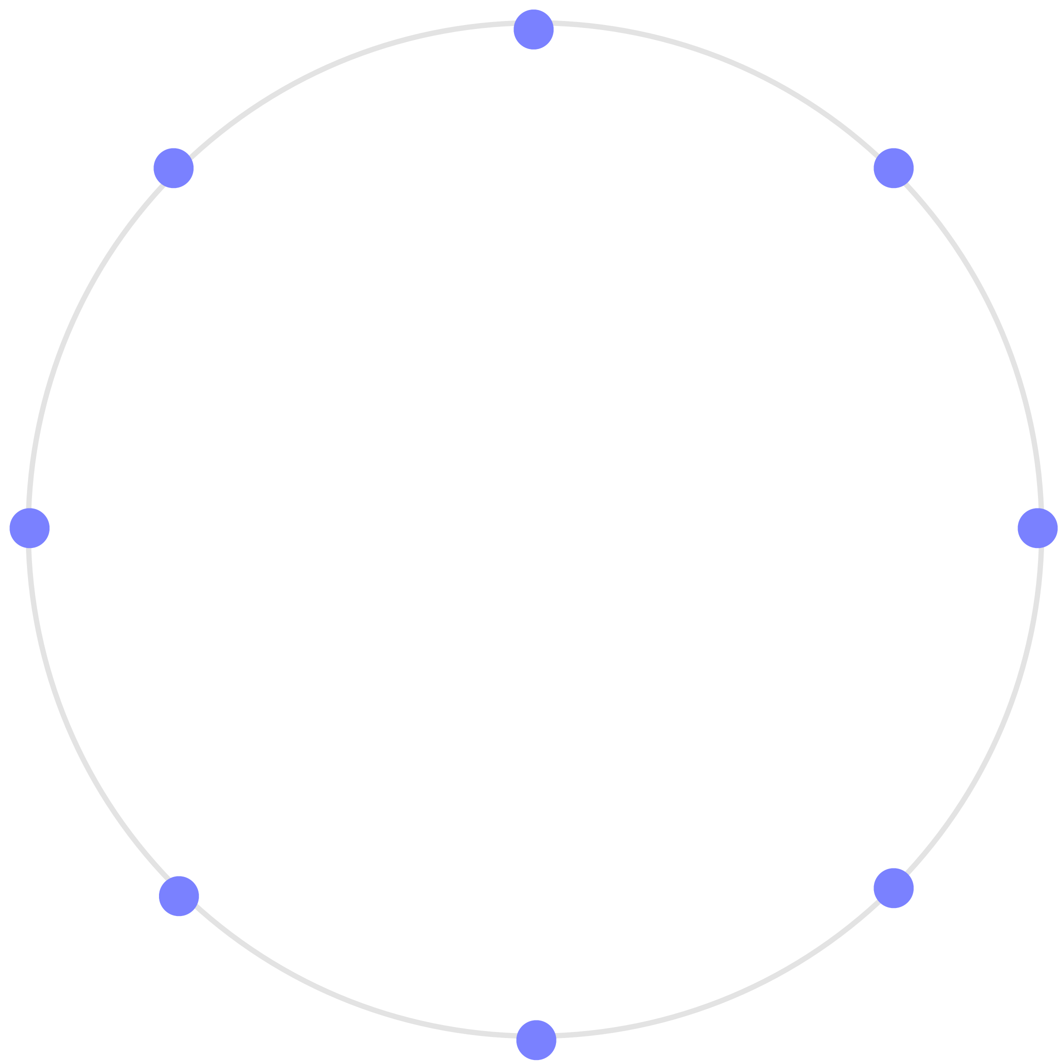
Abstraction

Values on the n wires are points in the n-dimensional space

Comparators are hyperplanes distinguishing points

3 Bits
2 Wires

3 Bits
2 Wires



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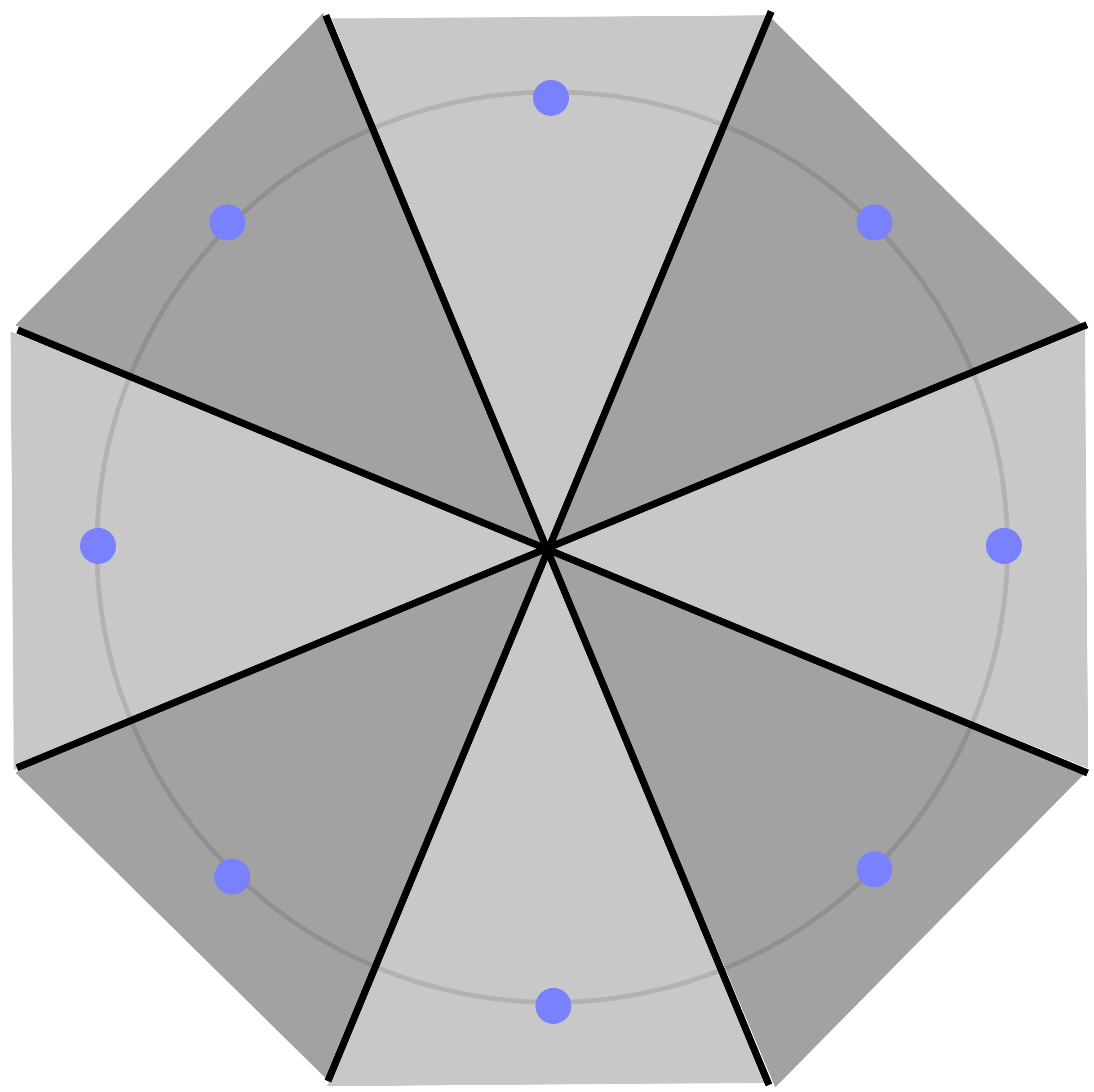

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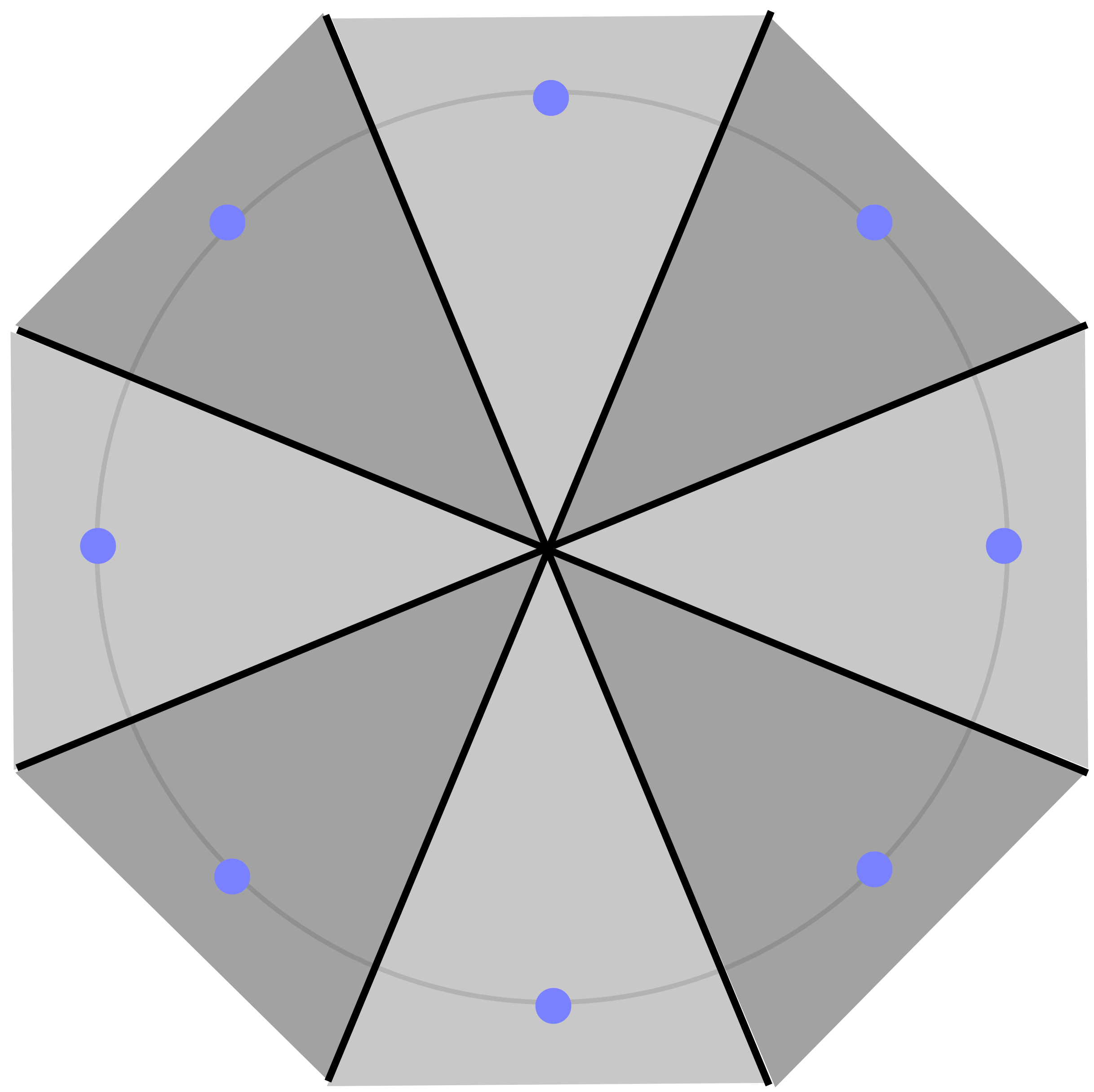

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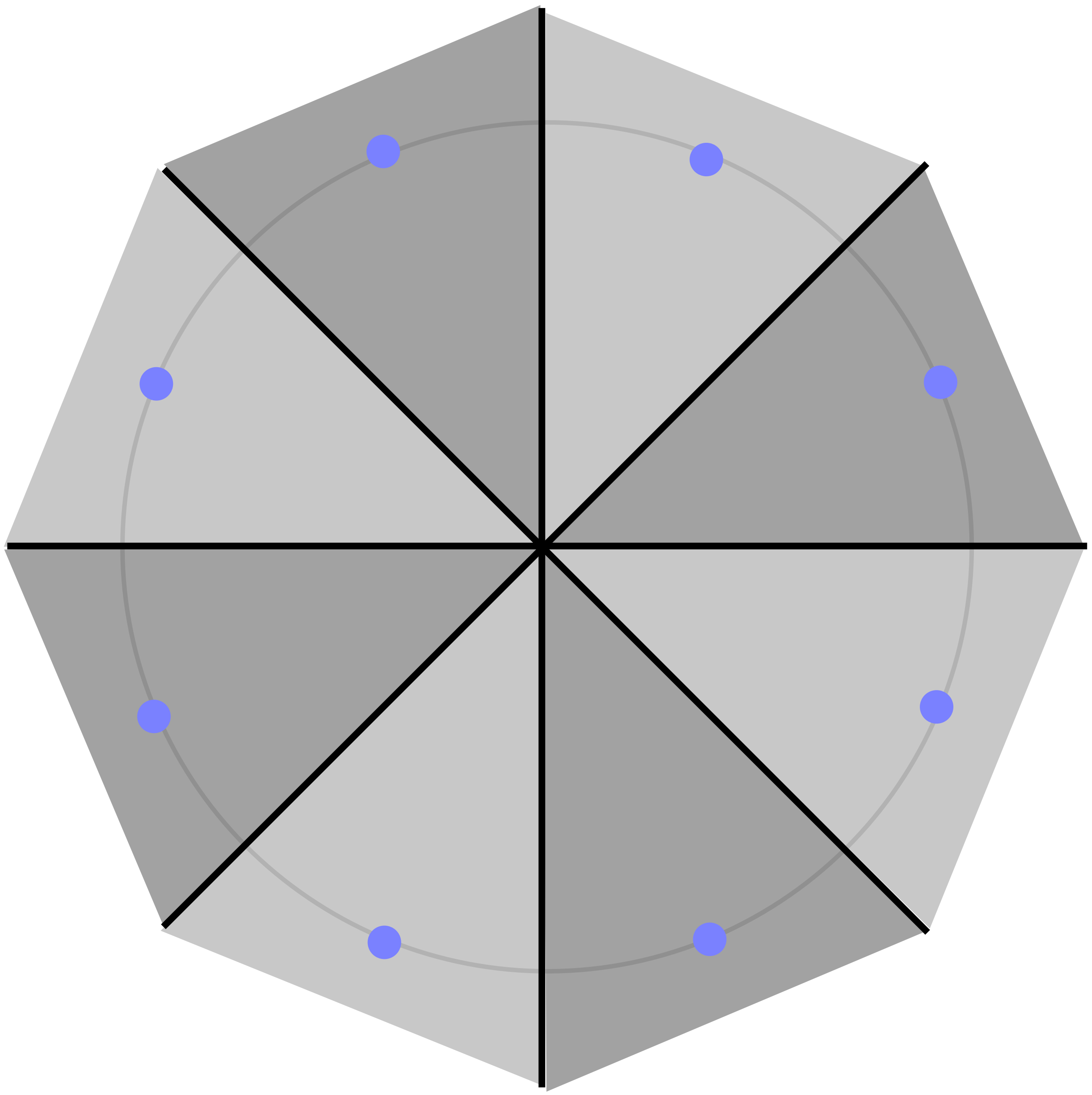

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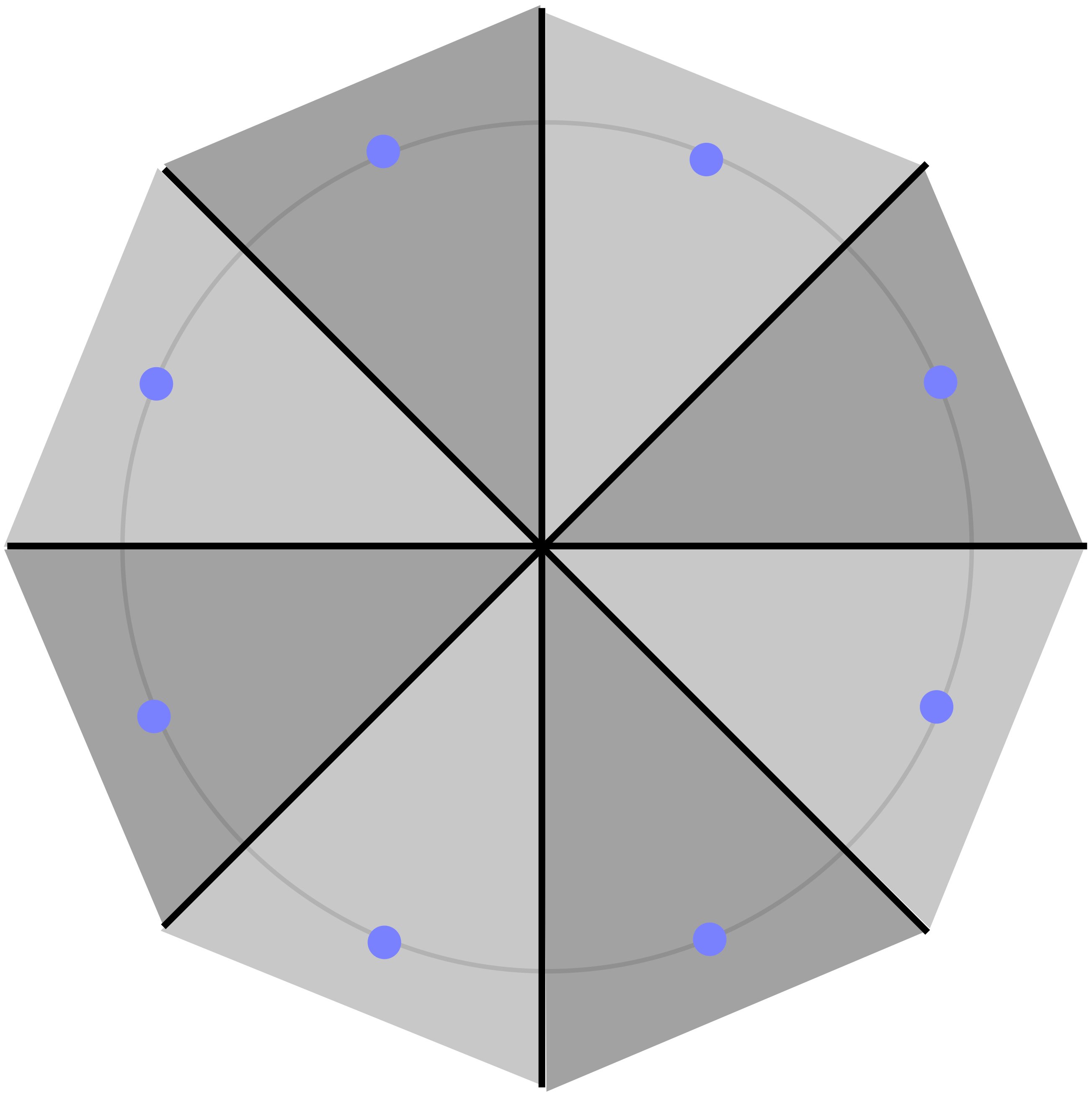

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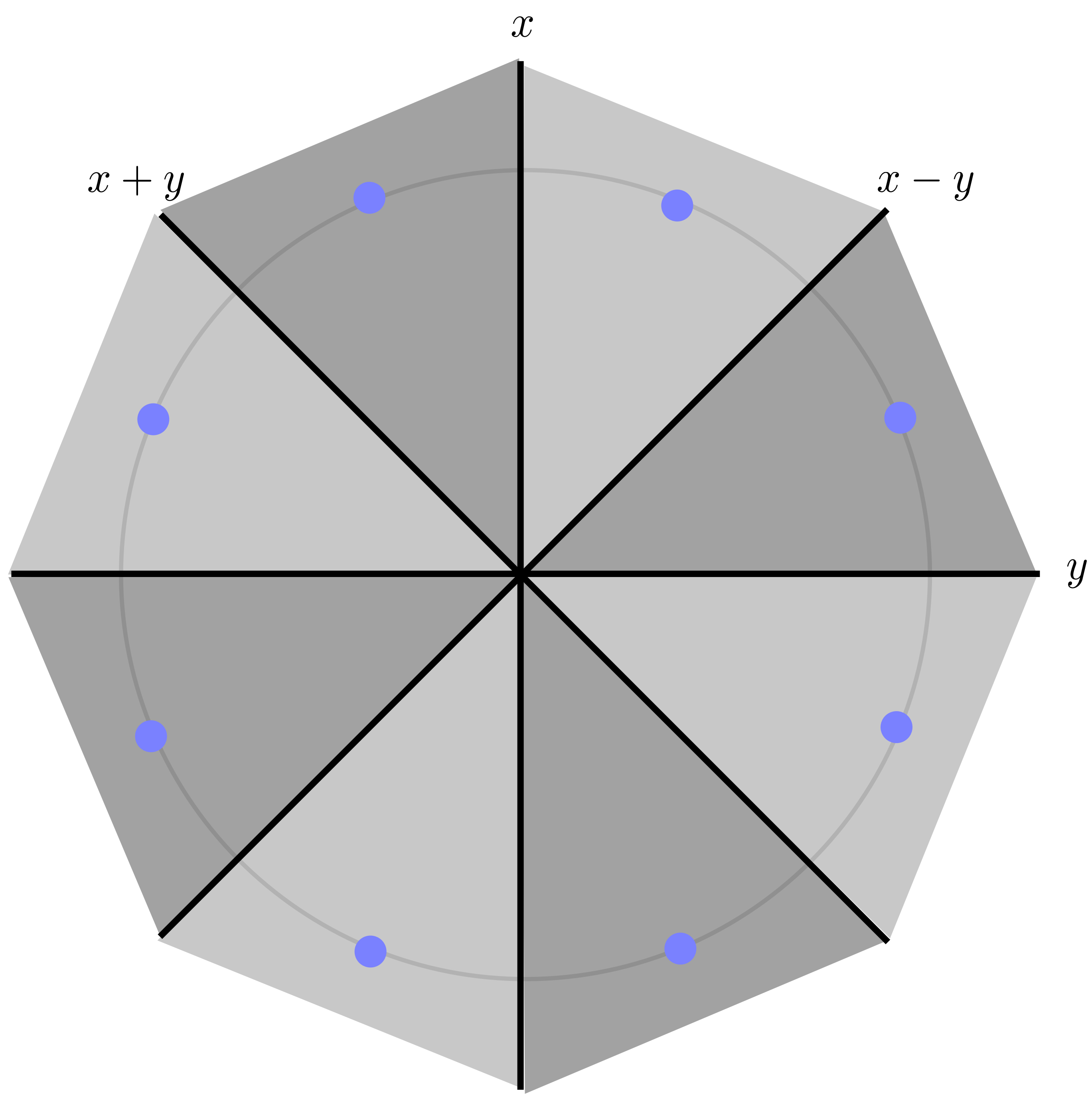

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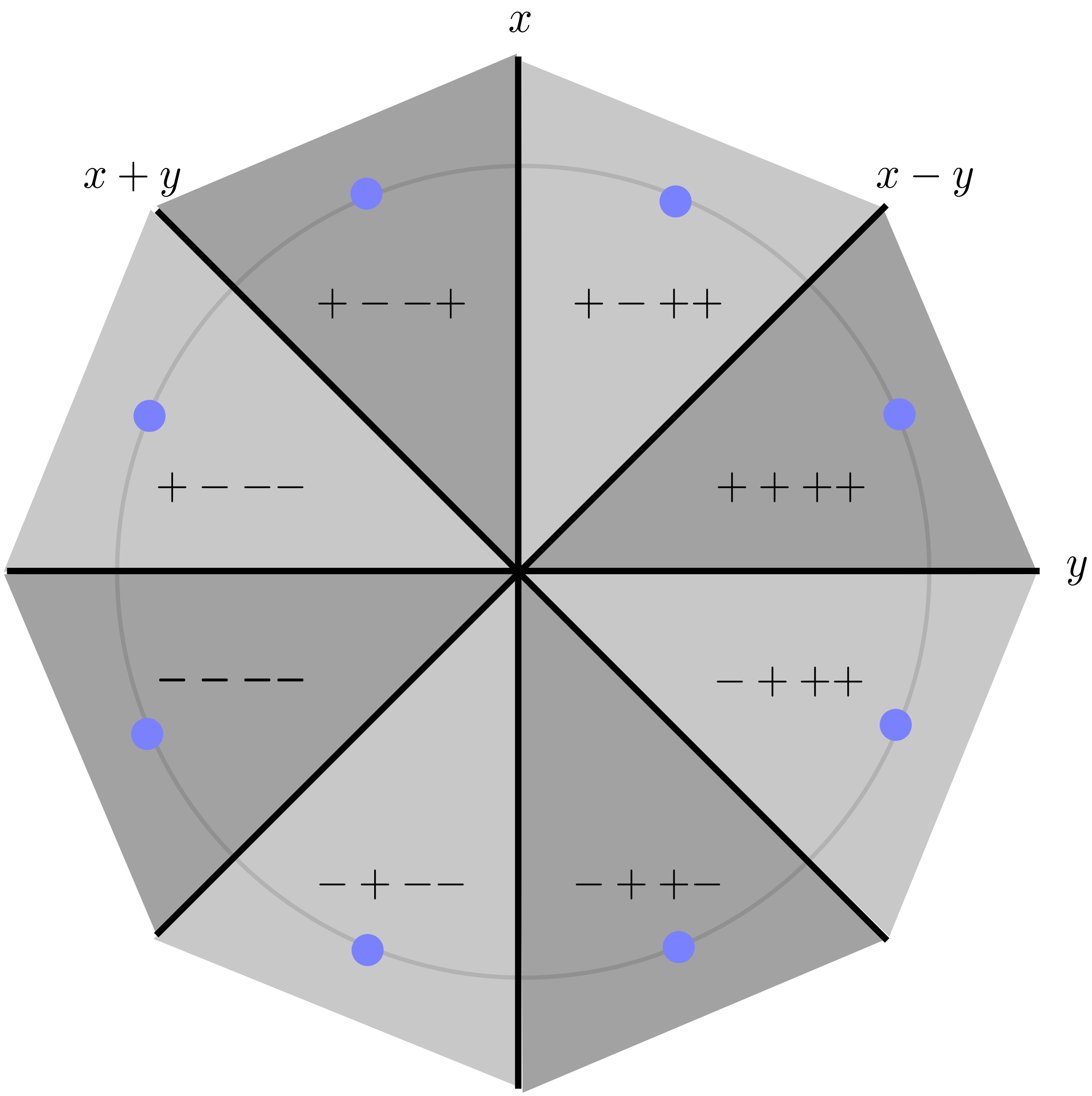

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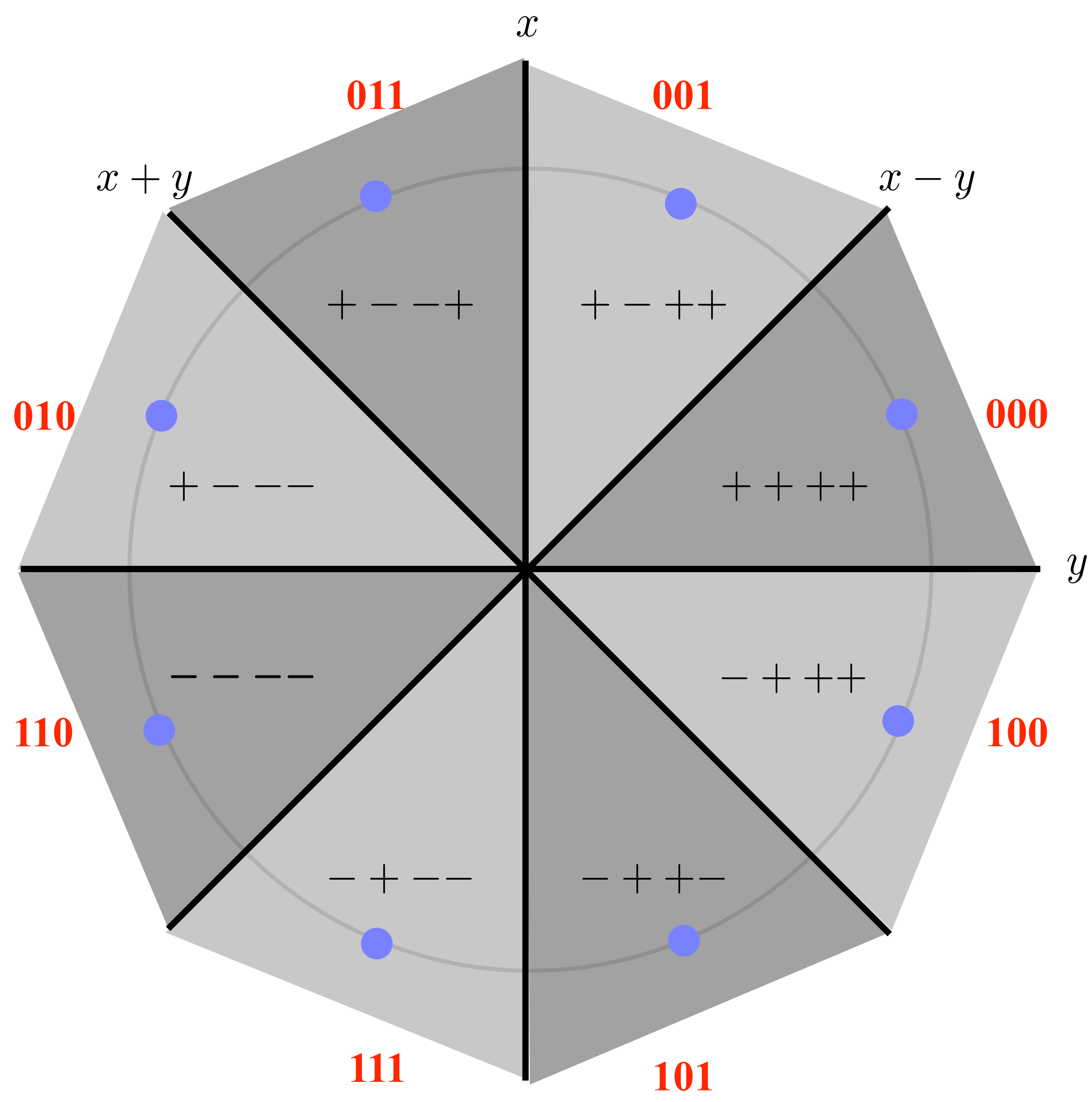
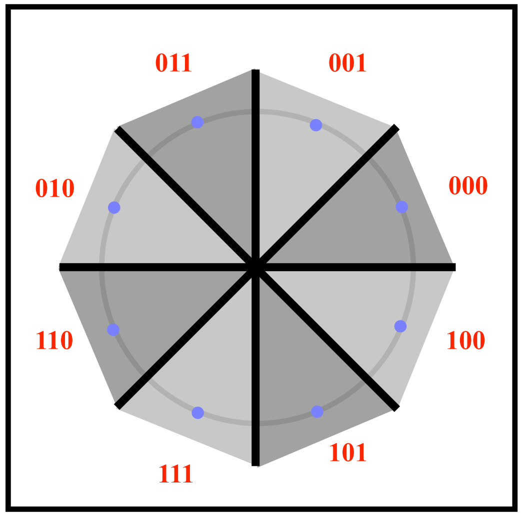


Driver, Encoder



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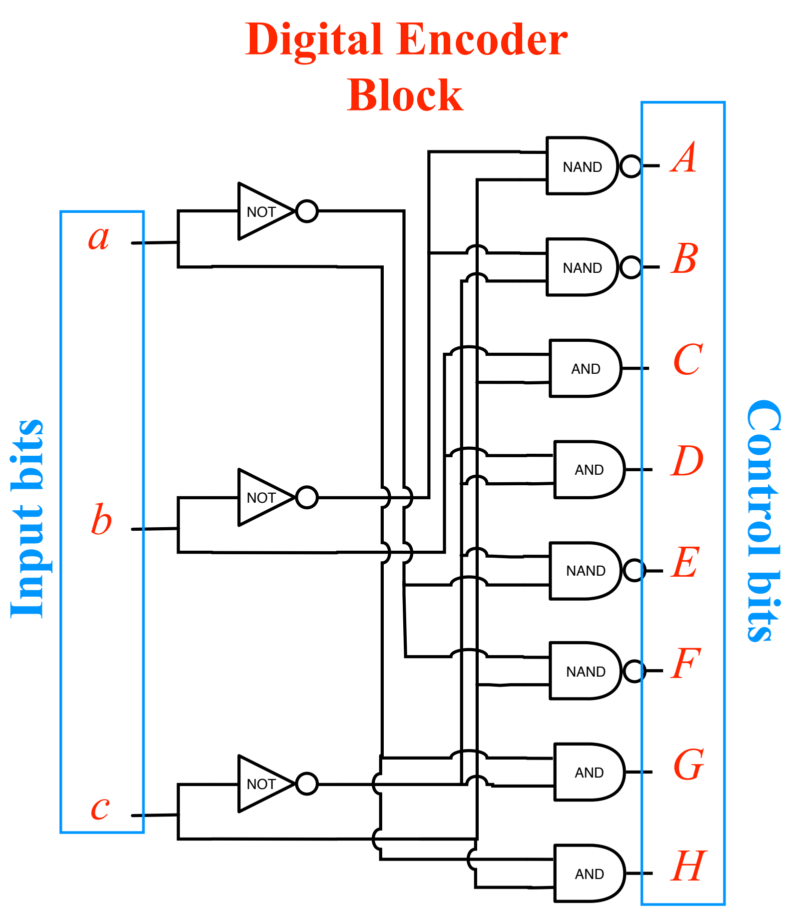

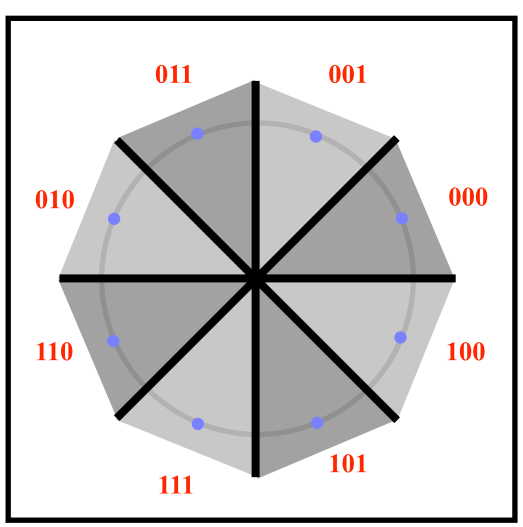

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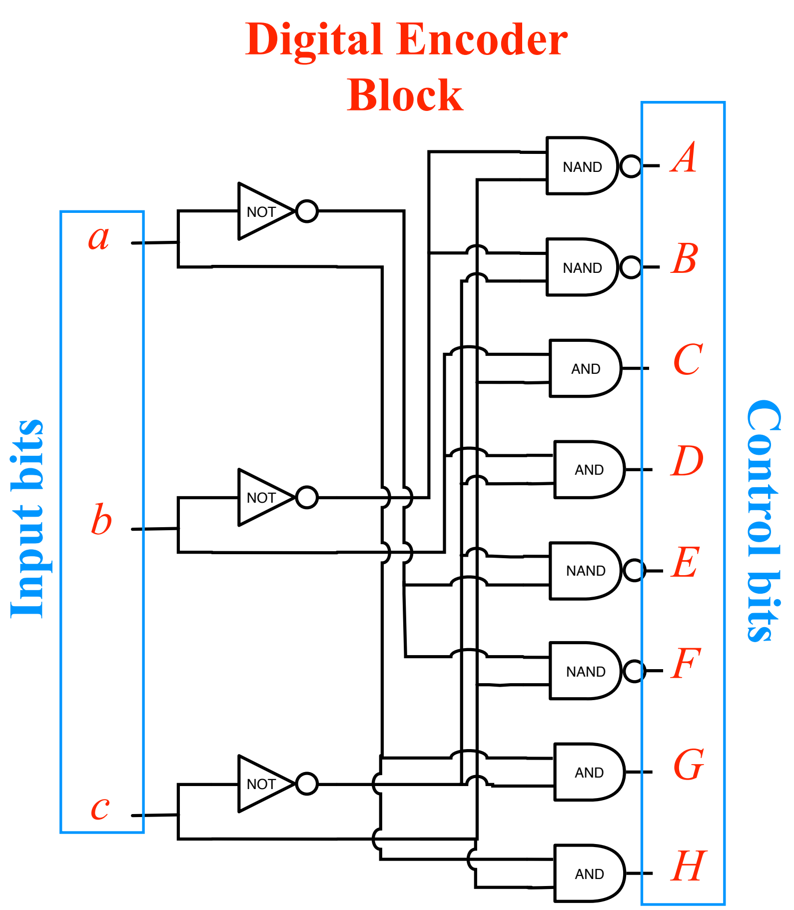

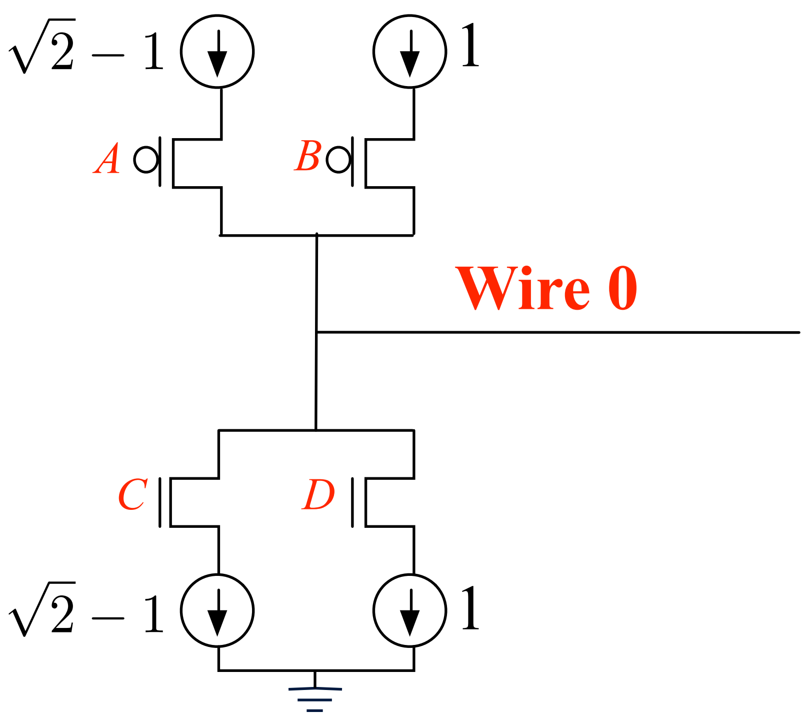

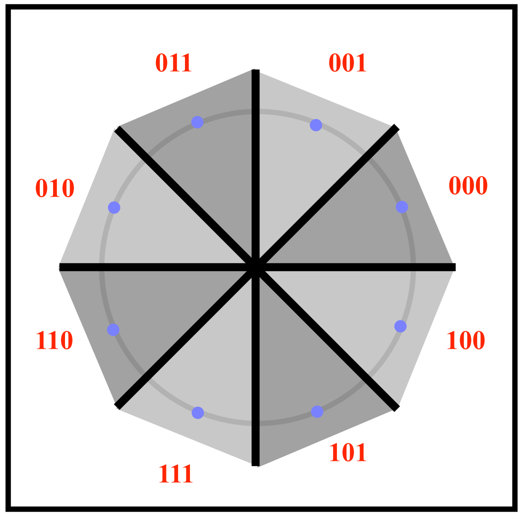

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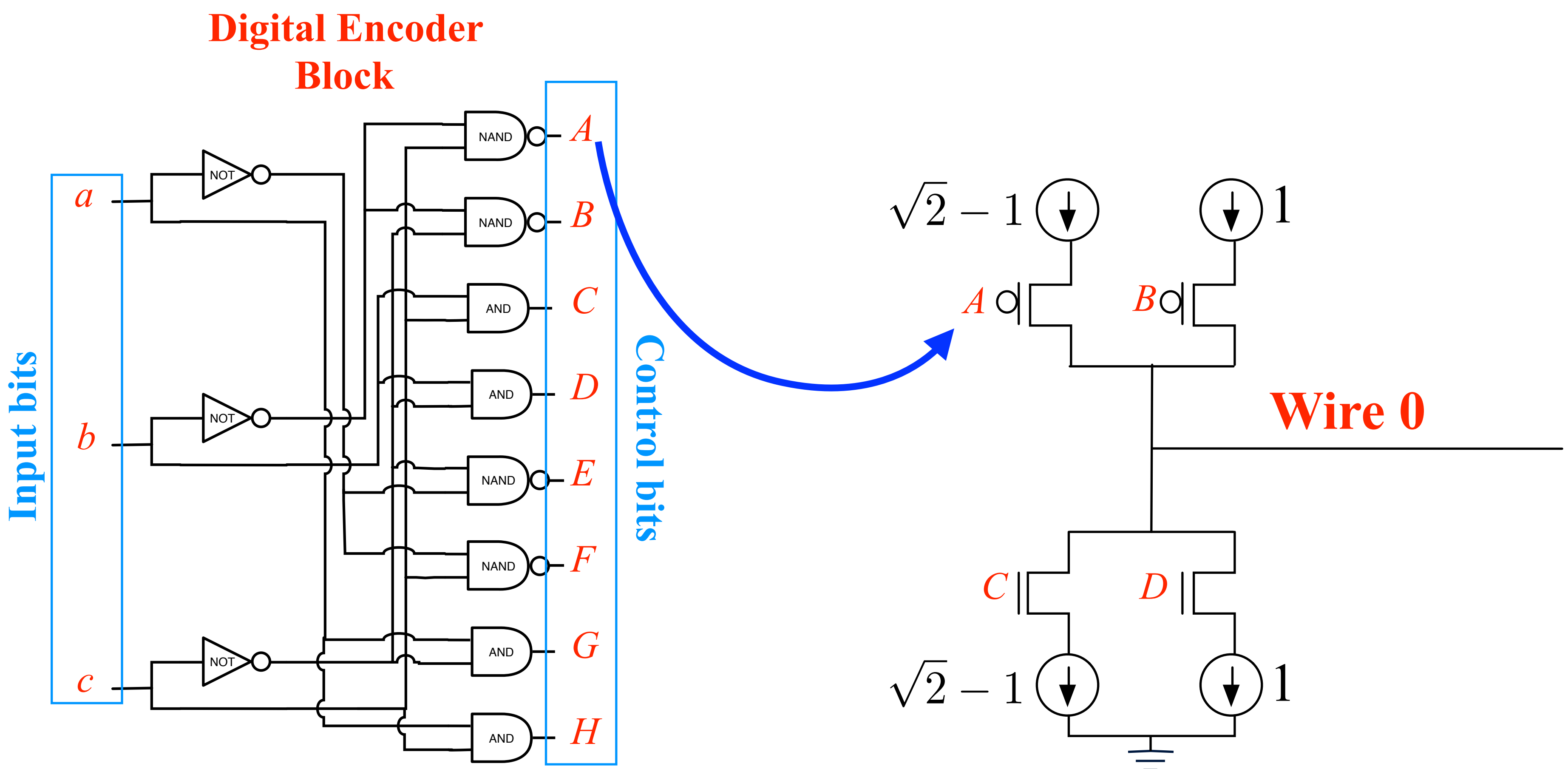

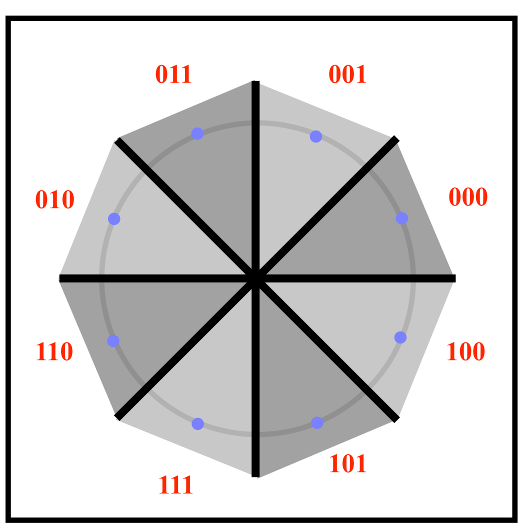

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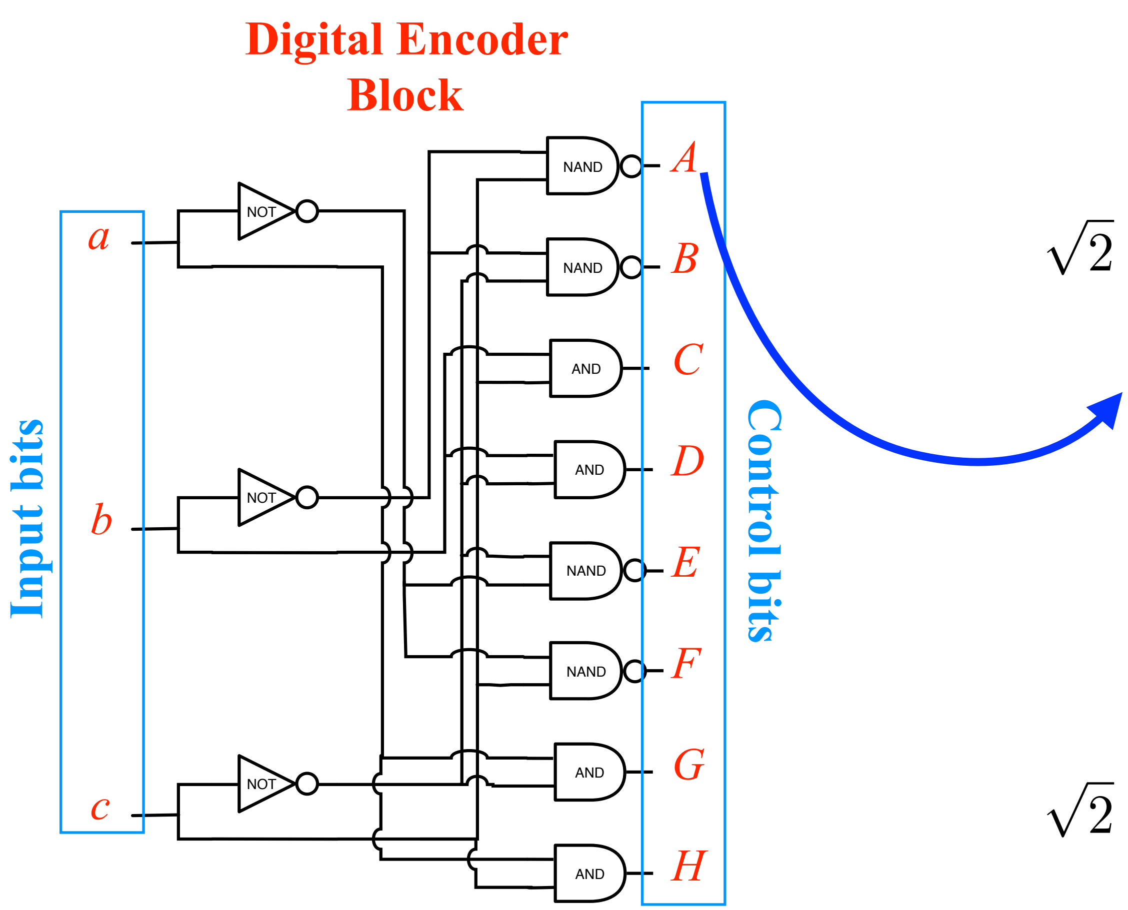

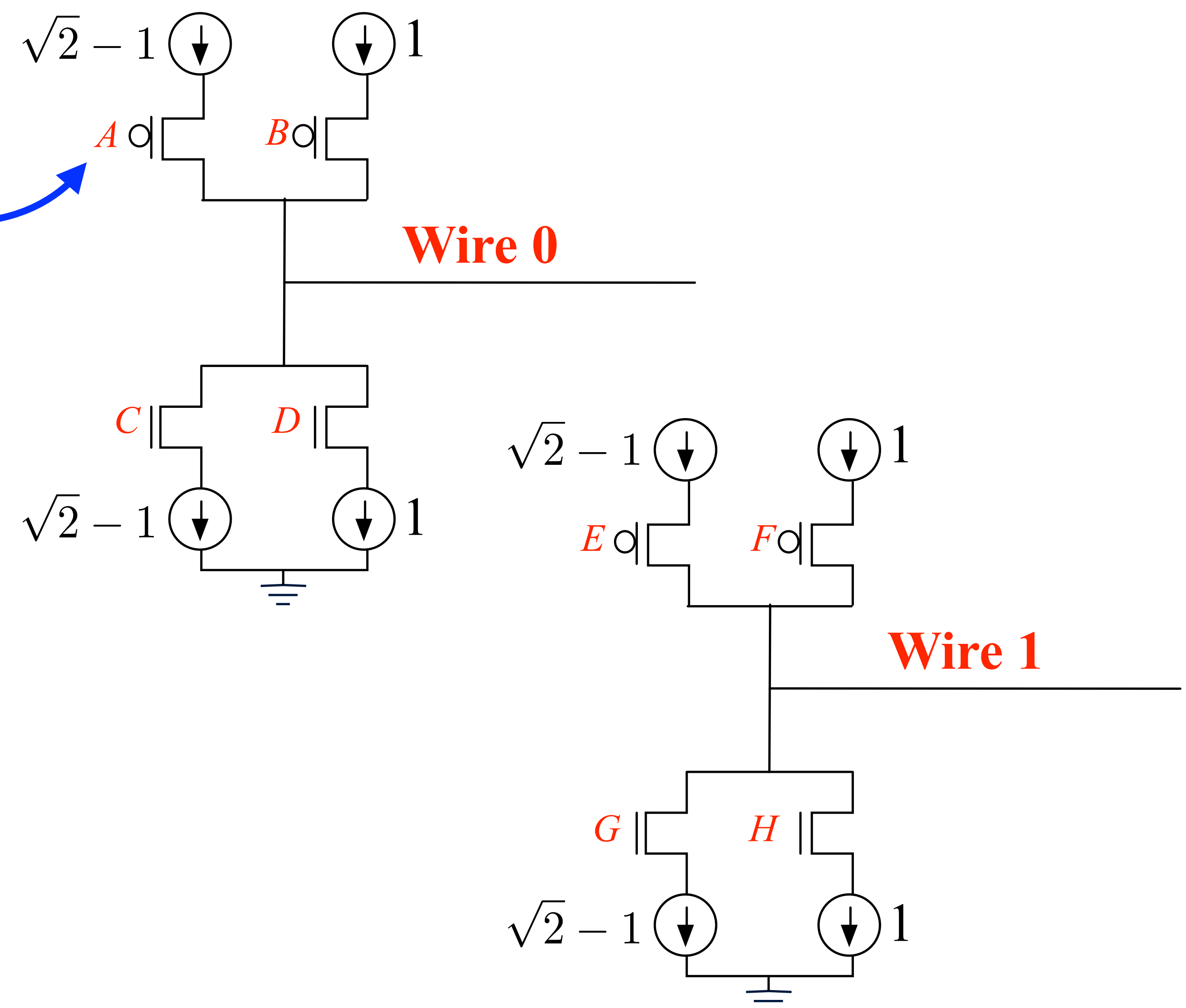

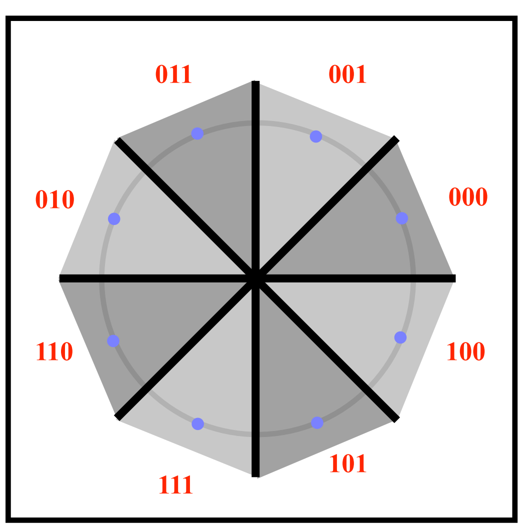

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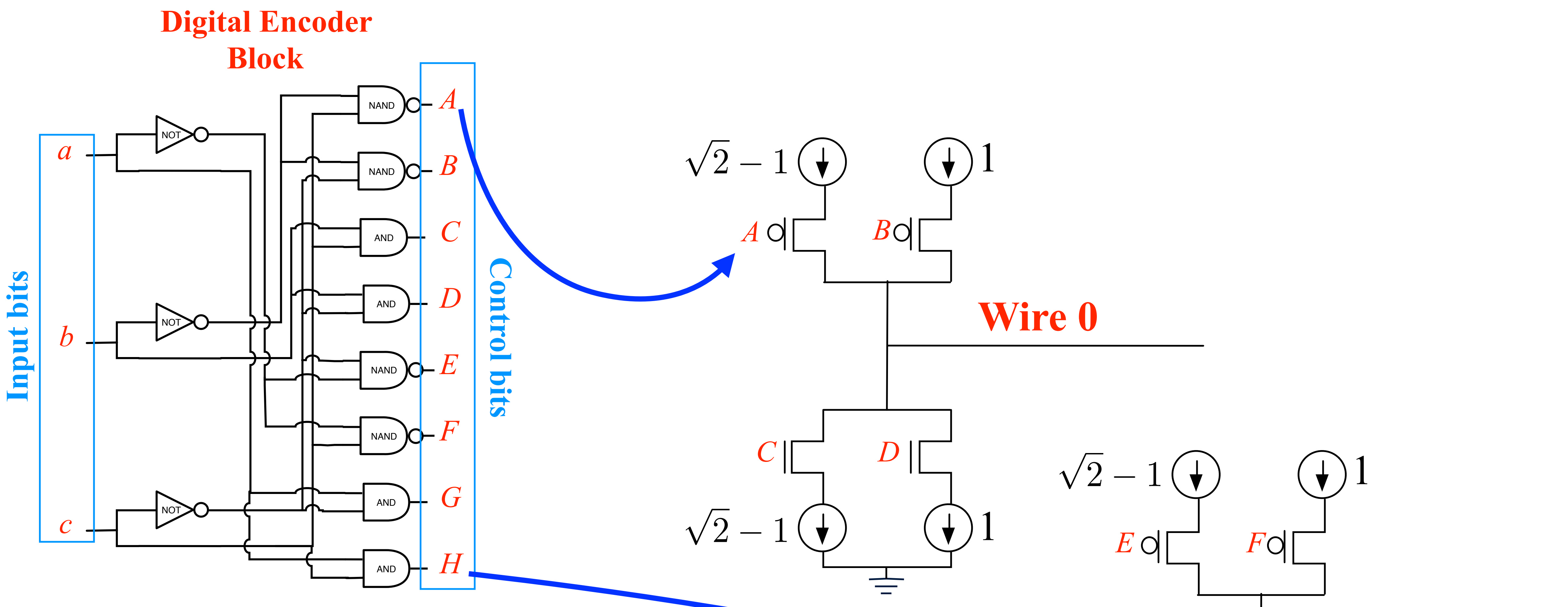
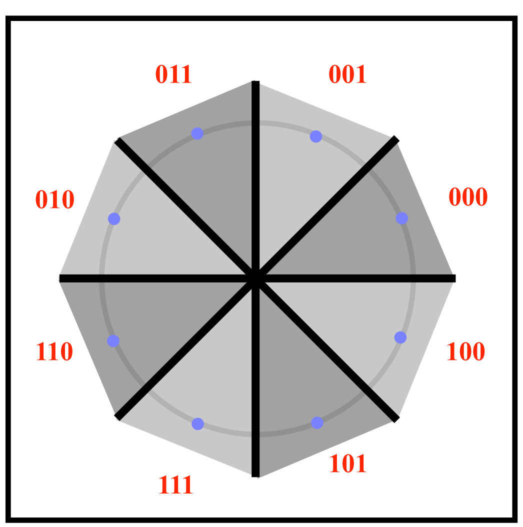
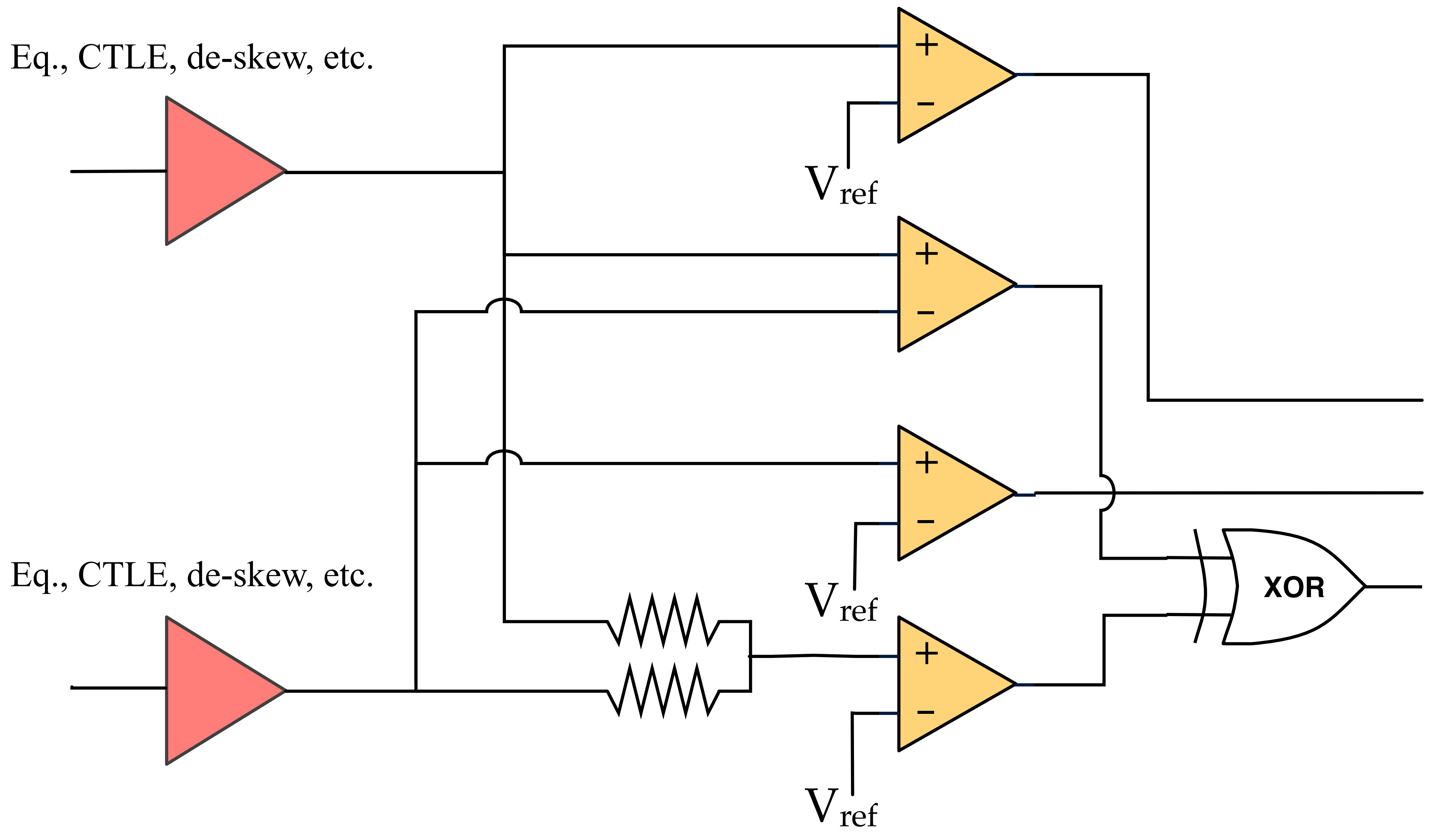
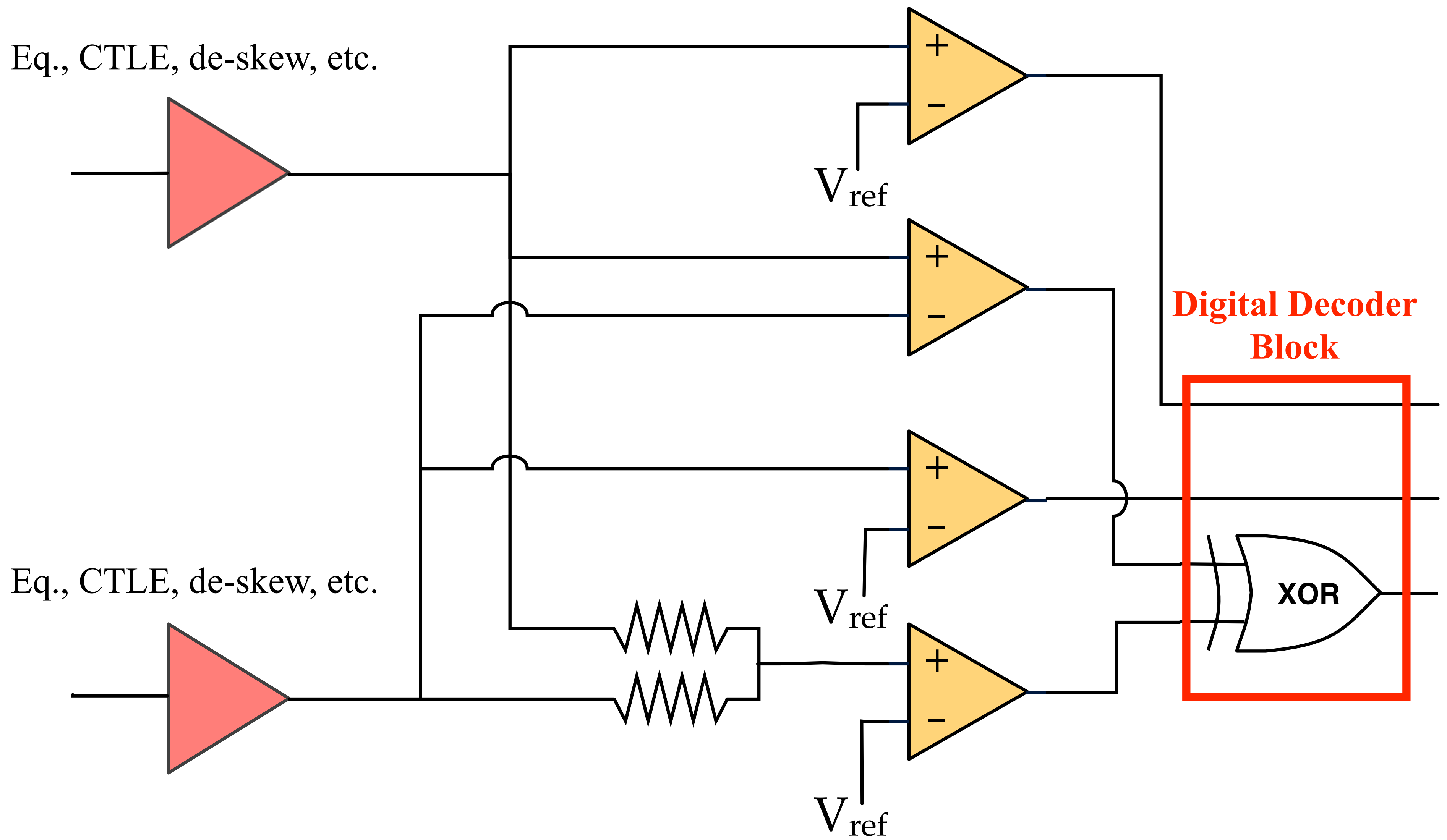




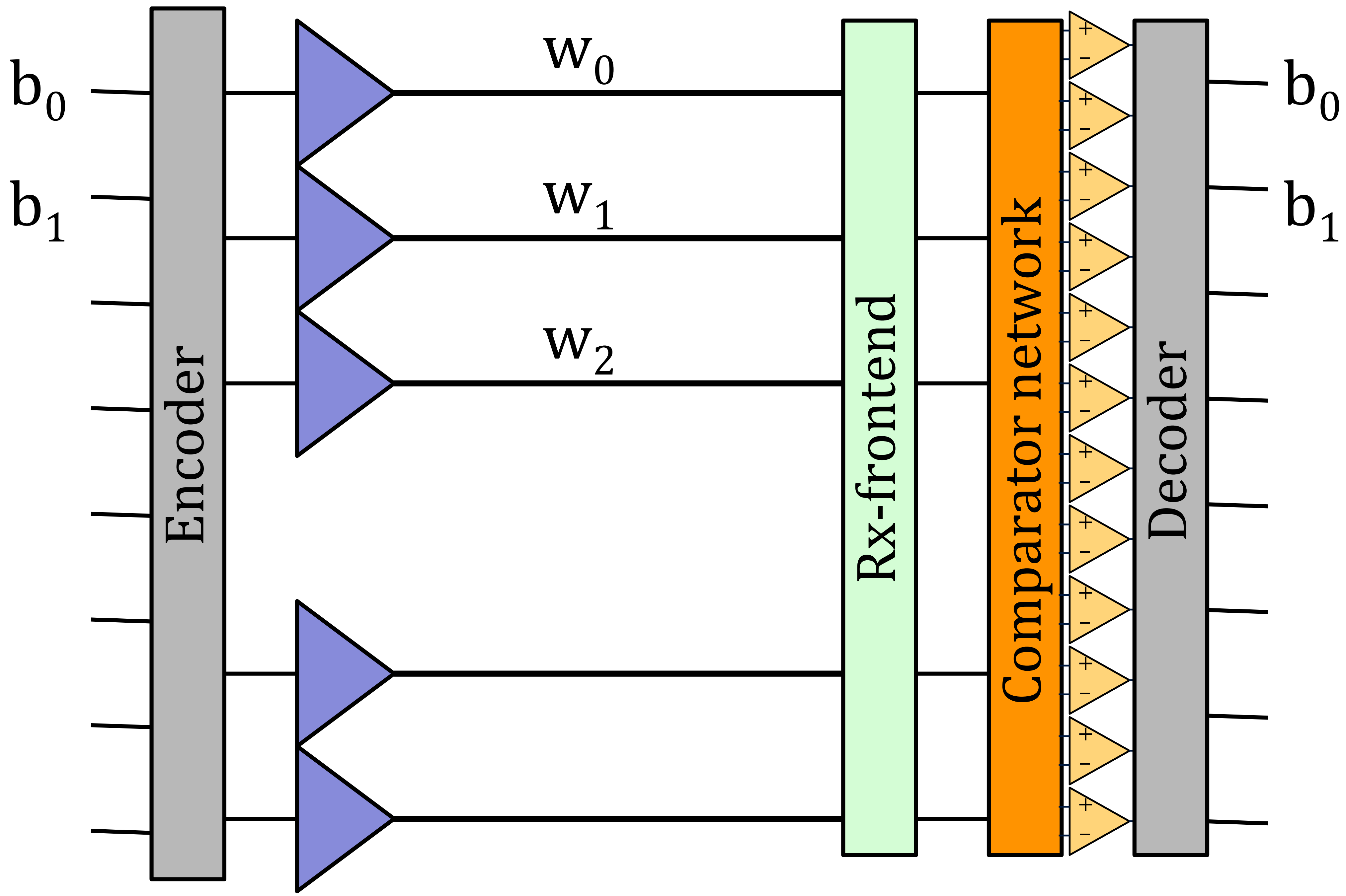
Receiver, Decoder



Receiver, Decoder



General Architecture



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Parameters

- n is the interface size, i.e., number of wires in the interface.
  - n = dimension of space we are operating in.

- c = number of comparators = number of hyperplanes used to separate the points
  - All hyperplanes pass through origin (centrally referenced).

distinguish?

- **Zaslavsky's formula**: N is at most equal to $$\sum_{i=0}^{n-1}\binom{c}{i}\left(1+(-1)^{n-1-i}\right)$$

Parameters

- n is the interface size, i.e., number of wires in the interface.
  - n = dimension of space we are operating in.
- c = number of comparators = number of hyperplanes used to separate the points
  - All hyperplanes pass through origin (centrally referenced).
- What is the maximum number N of chambers of this arrangement?
  - Equivalently, what is the maximum number of points we can distinguish?
- **Zaslavsky's formula**: N is at most equal to $$\sum_{i=0}^{n-1} \binom{c}{i} \left(1 + (-1)^{n-1-i}\right)$$

Examples

c = # comparators = # hyperplanes

n = # wires

	2	3	4	5	6	7	8	9	10	11	12	13
2	4	6	8	10	12	14	16	18	20	22	24	26
3	4	8	14	22	32	44	58	74	92	112	134	158
4	4	8	16	30	52	84	128	186	260	352	464	598
5	4	8	16	32	62	114	198	326	512	772	1124	1588
6	4	8	16	32	64	126	240	438	764	1276	2048	3172
7	4	8	16	32	64	128	254	494	932	1696	2972	5020
8	4	8	16	32	64	128	256	510	1004	1936	3632	6604

Possible to transmit 7 bits on 4 wires with a detector using 8 comparators

But....

What happens to noise?

Noise

Chord signaling can help lower the frequency. Does it help?

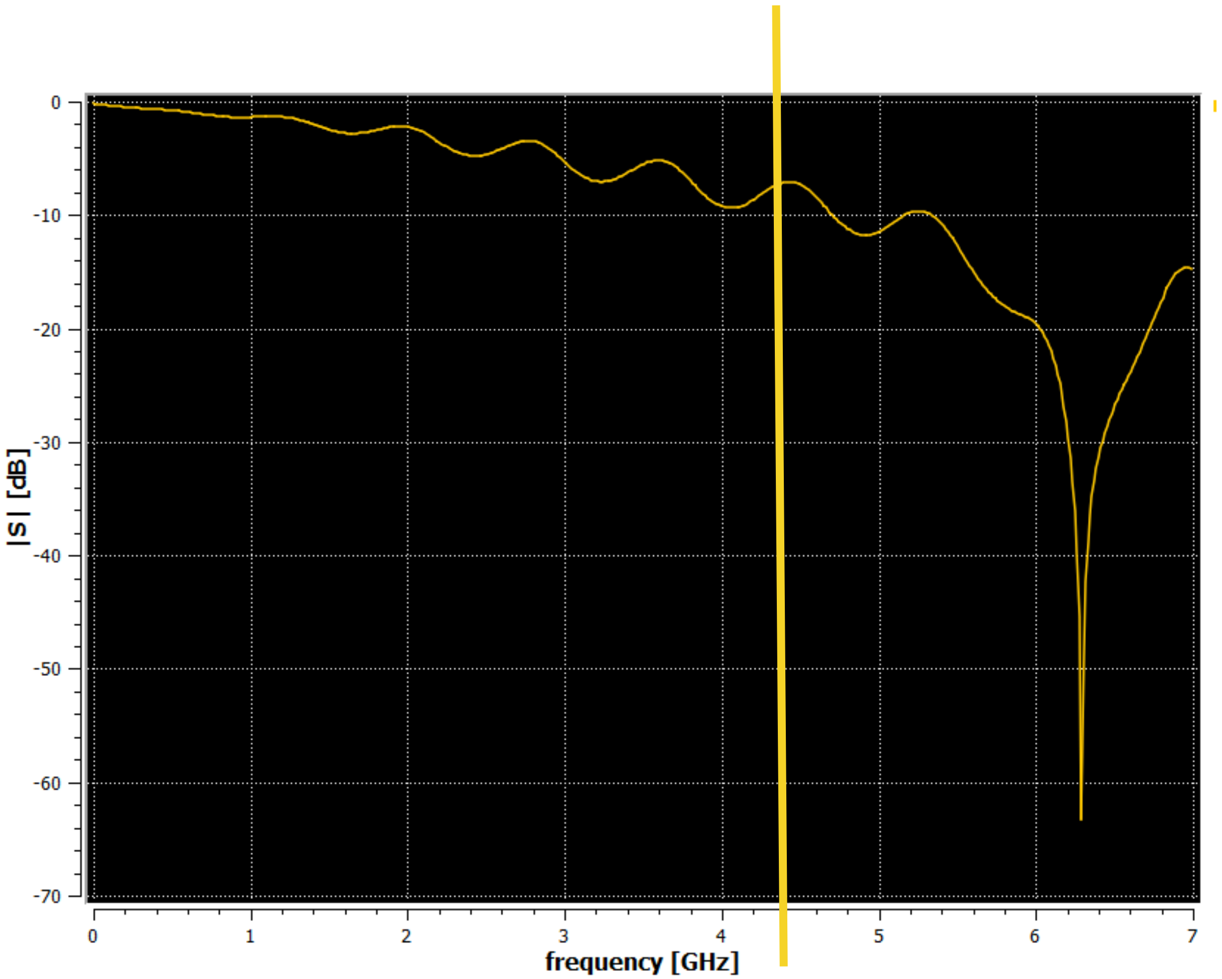
Noise

	Single-ended	Differential	4-PAM diff.	Chord Signaling (so far)
SSO	-	+	+/-	-
Ref	-	+	-	-
EMI	-	+	+	-
Common	-	+	+	-
ISI	+	-	- -	+/-
Conclusion	High speed problematic	Pin count problematic	High speed issues	May have issues

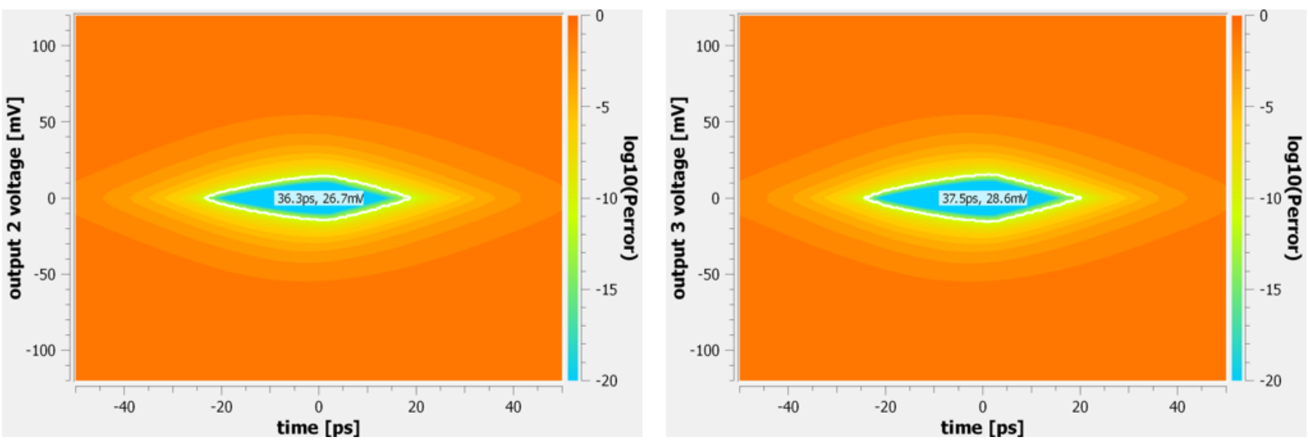
Chord signaling can help lower the frequency. Does it help?

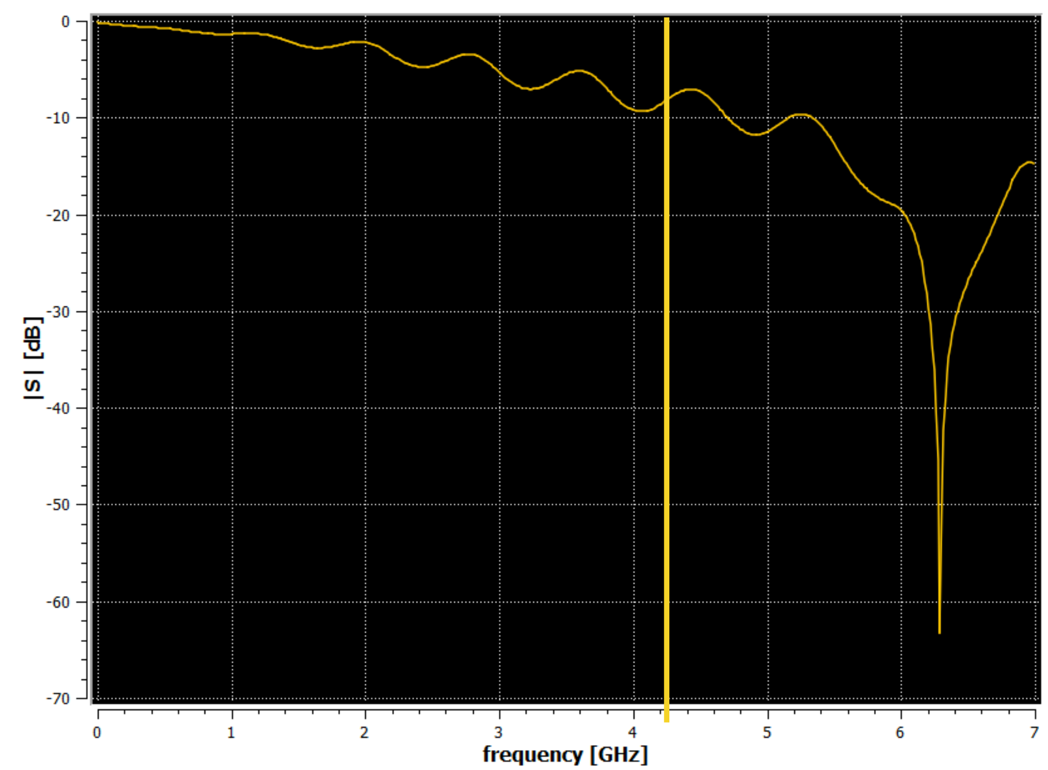
Simulations

- Realistic model of a mobile memory channel
- Channel consists of a group of 8 (9) wires
- Would like to transmit up to 8.4 Gbps/wire.
- Fundamental clock frequency is 4.2 GHz for single-ended signaling, corresponding to about 8 dB loss.



Statistical Eyes

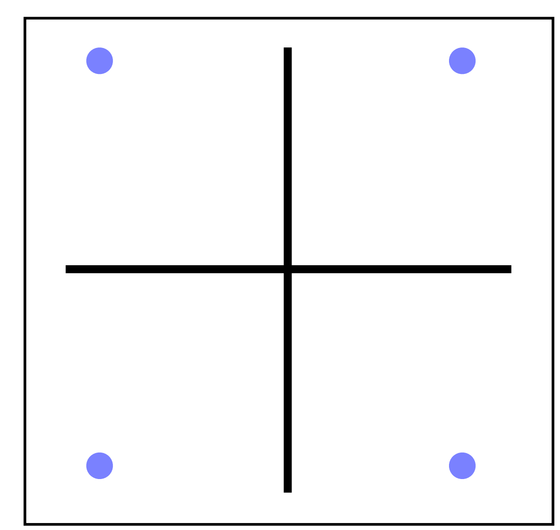




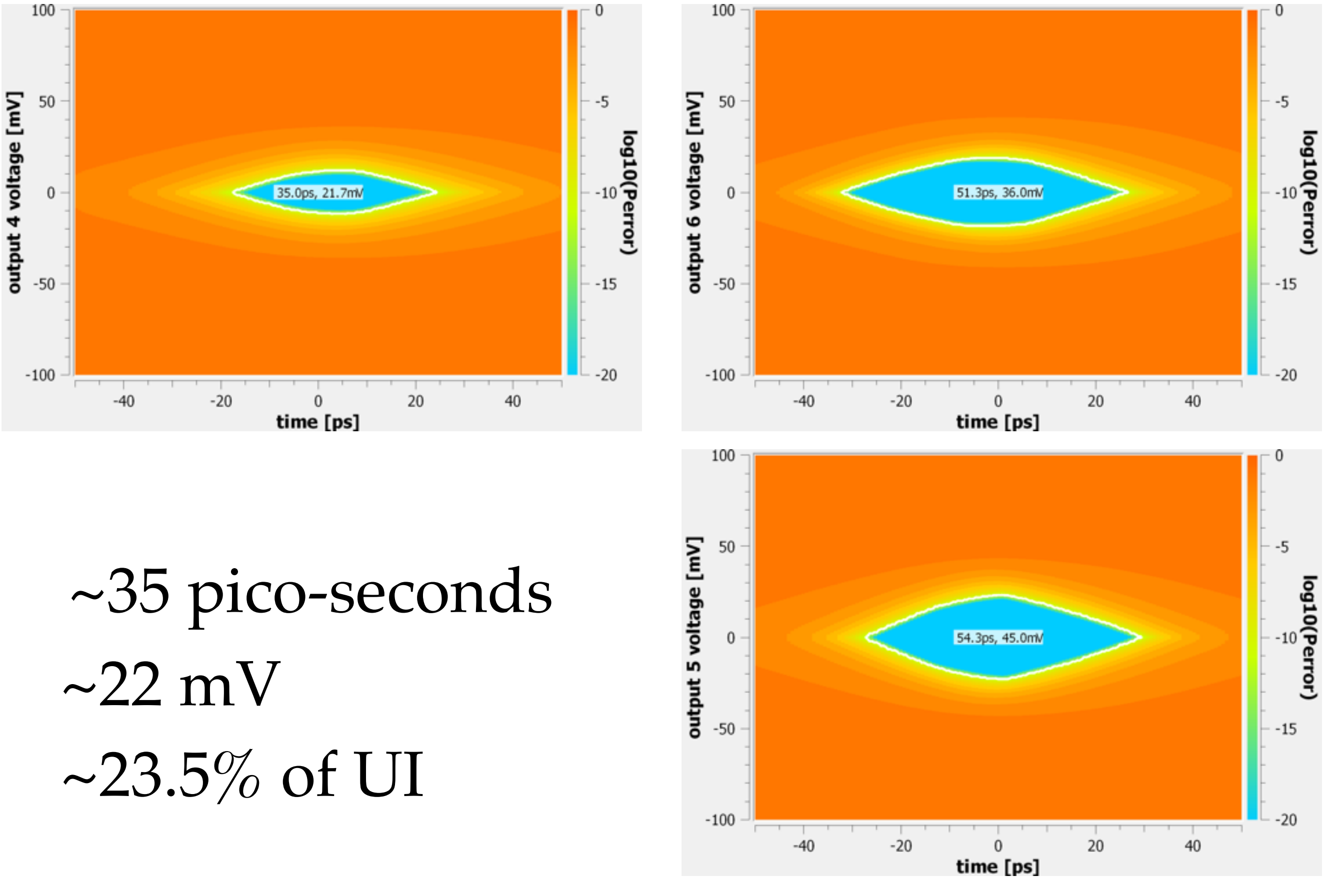
~36 pico-seconds

~27 mV

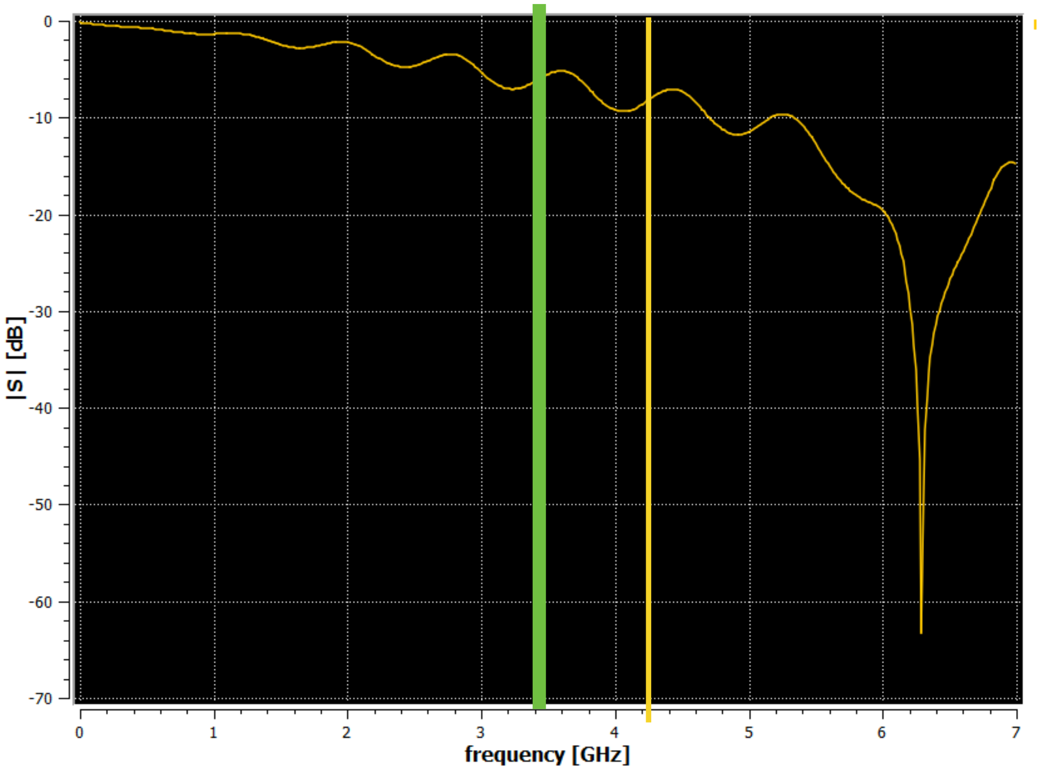
~30% of UI

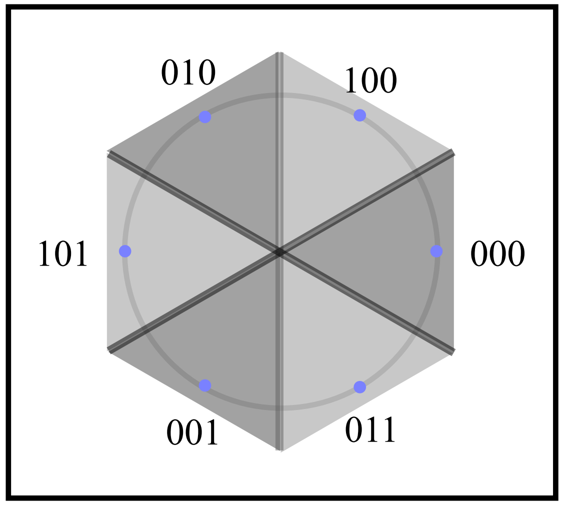


Statistical Eyes

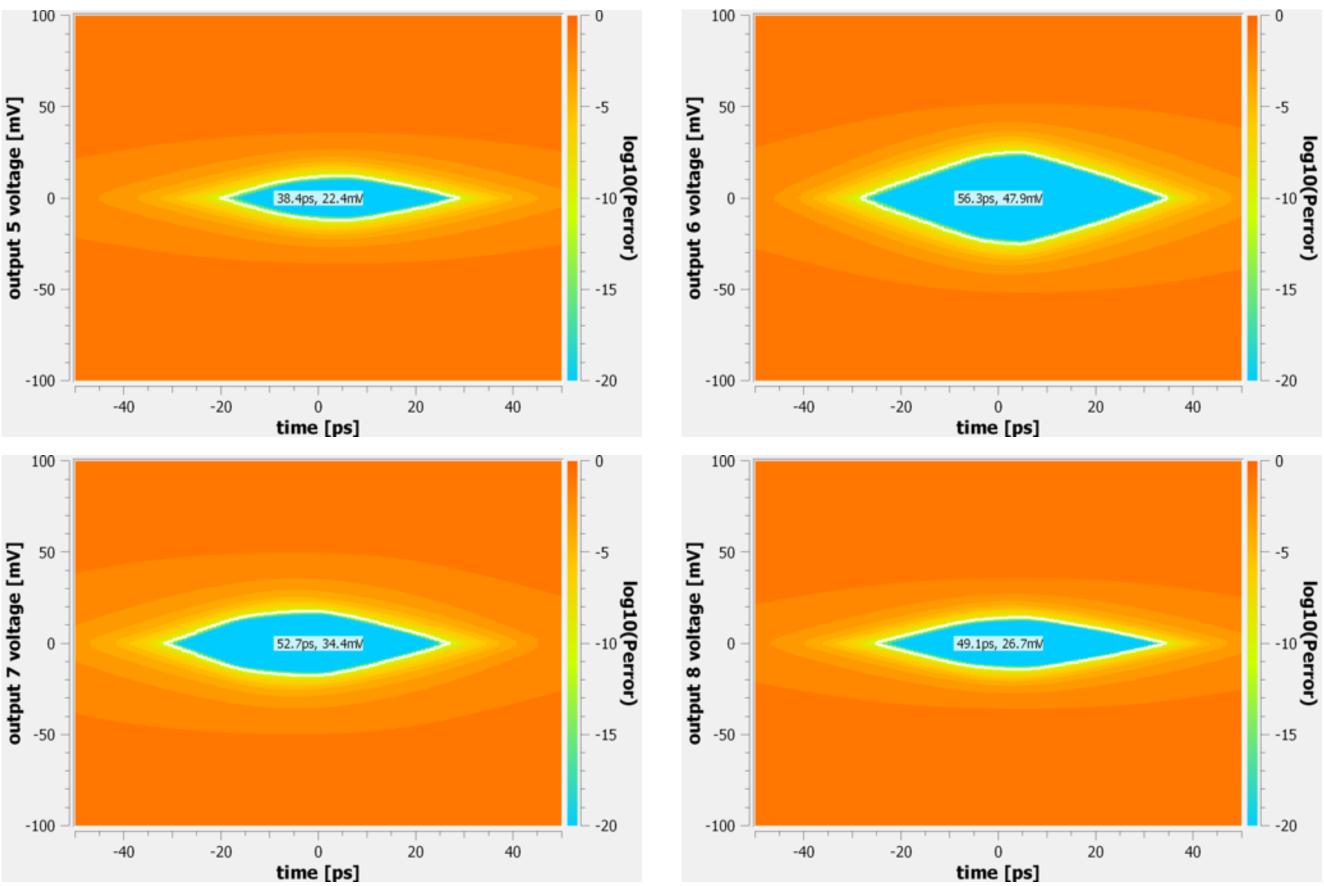


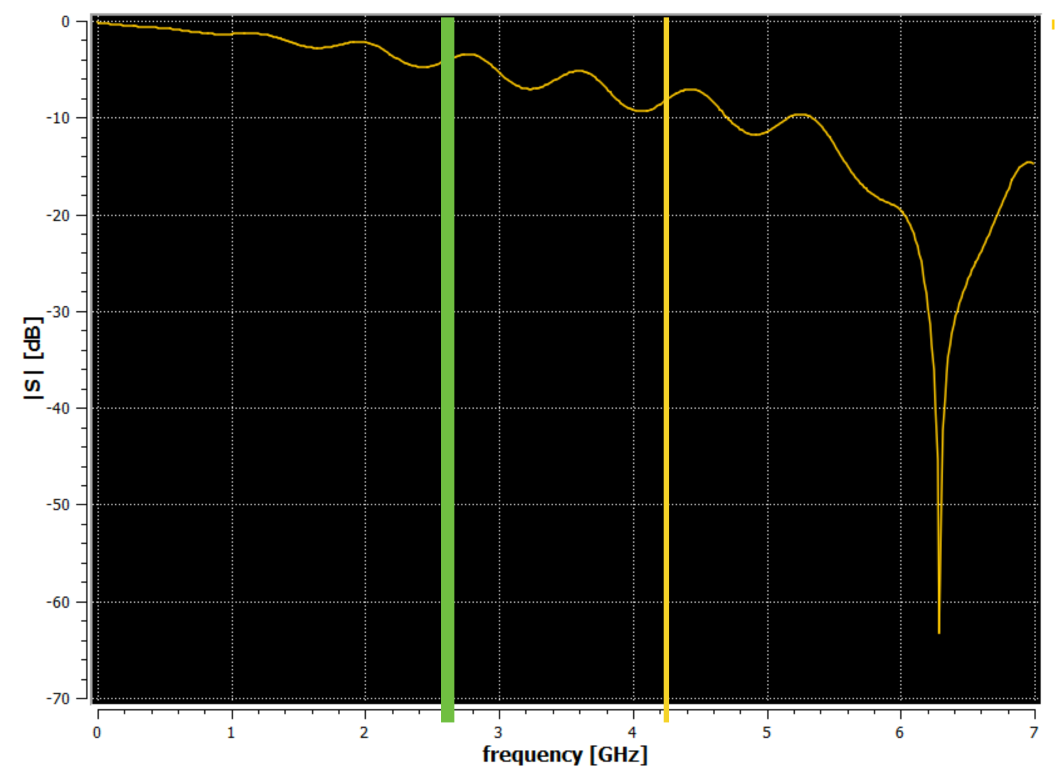
~35 pico-seconds
~22 mV
~23.5% of UI

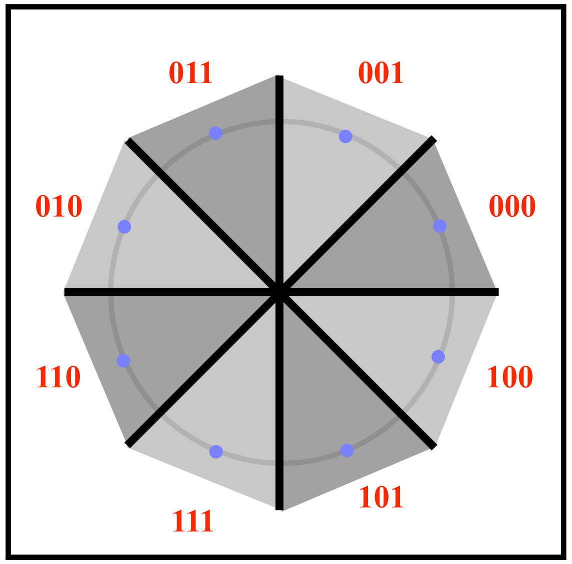




Statistical Eyes





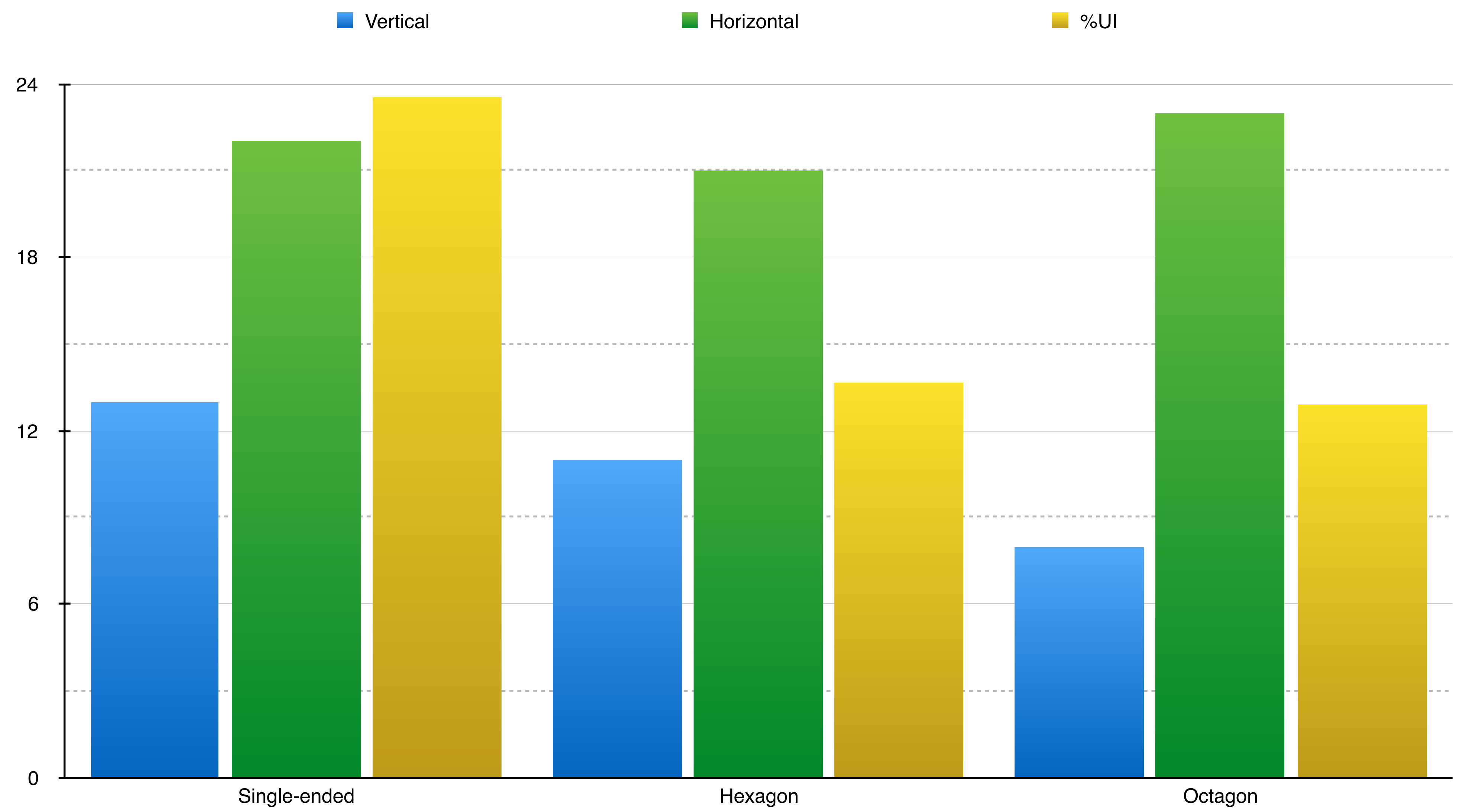


~38 pico-seconds

~22 mV

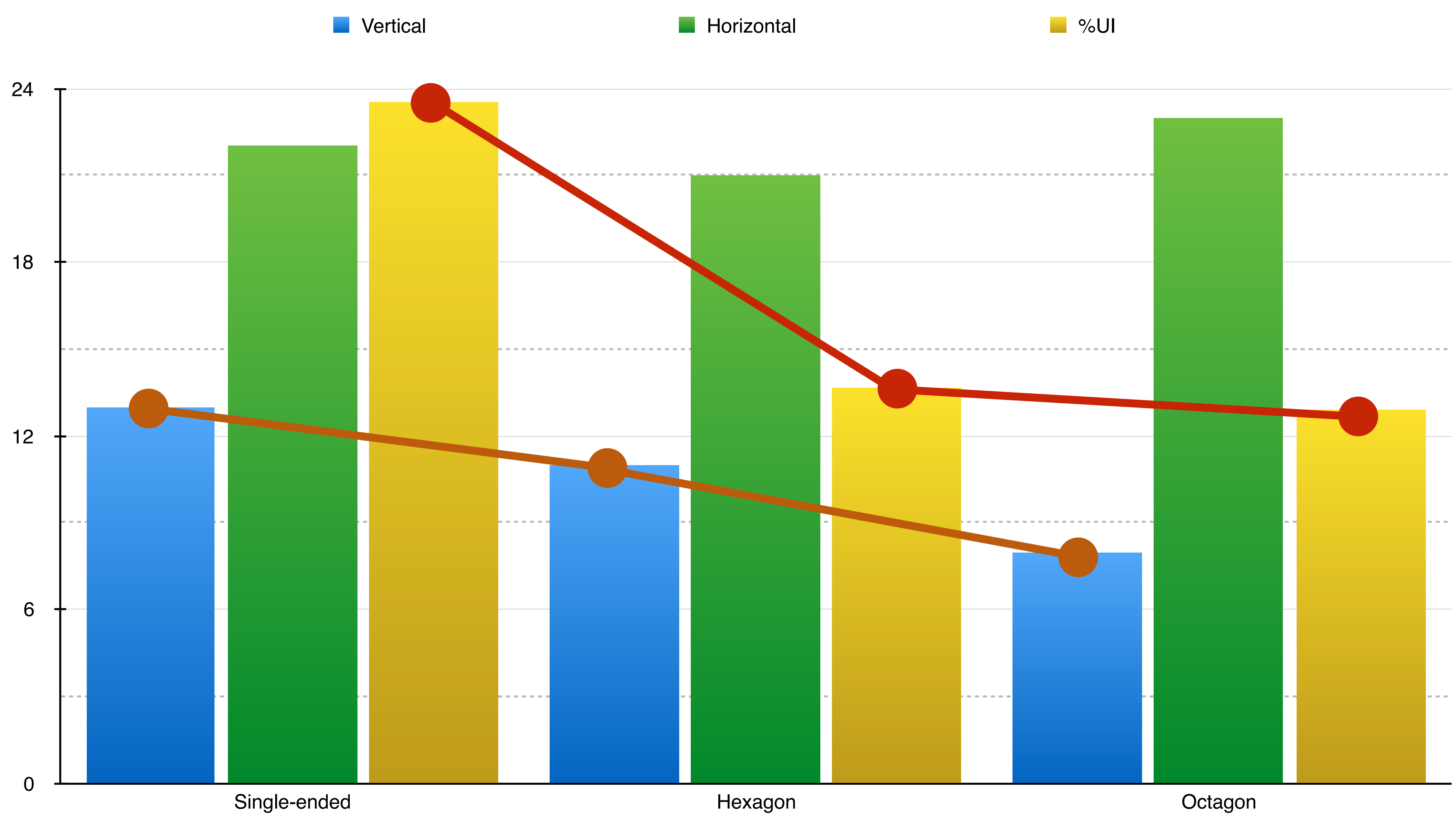
~21.5% of UI

Comparison



Vertical
Horizontal
%UI
24
18
12
6
0
Single-ended
Hexagon
Octagon

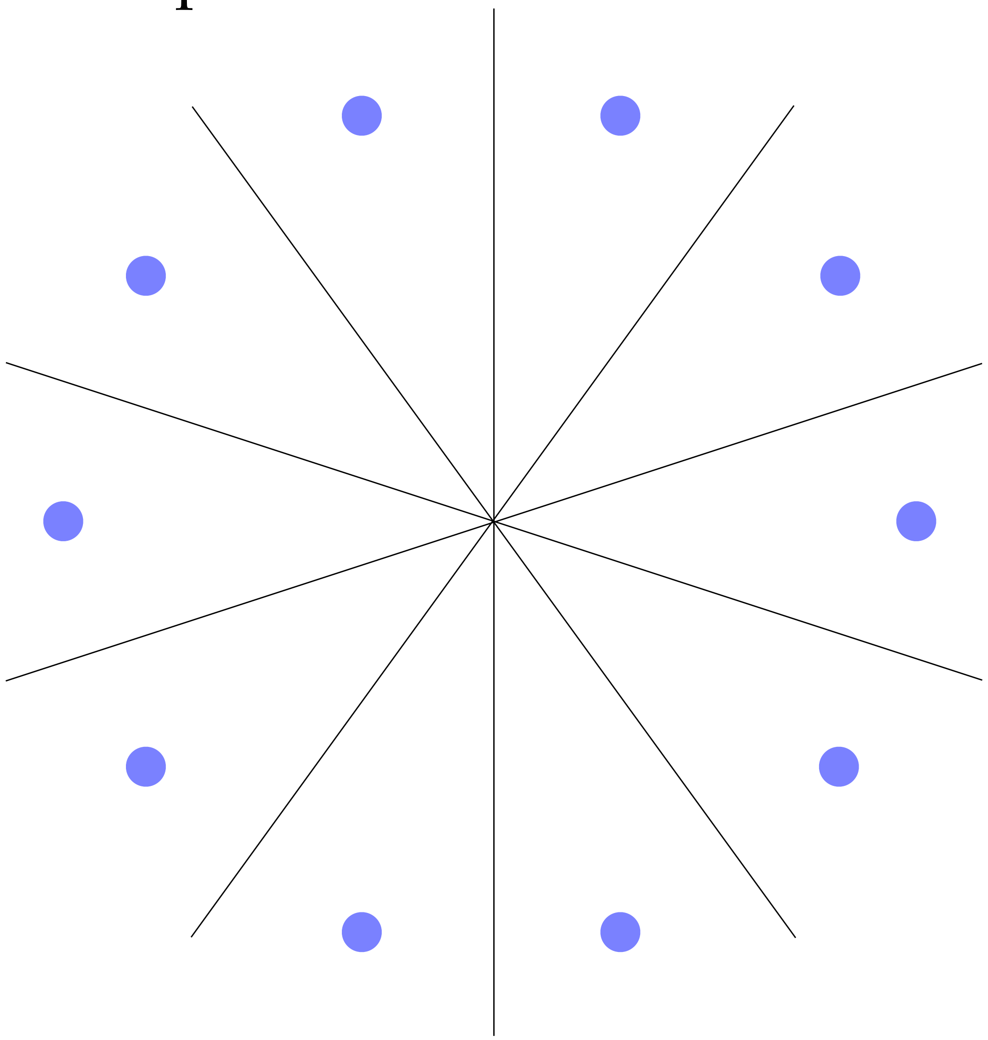
Comparison



Lowering the frequency didn’t really help

What is Happening?

- Chambers become very small when number increases
- System becomes more susceptible to noise.



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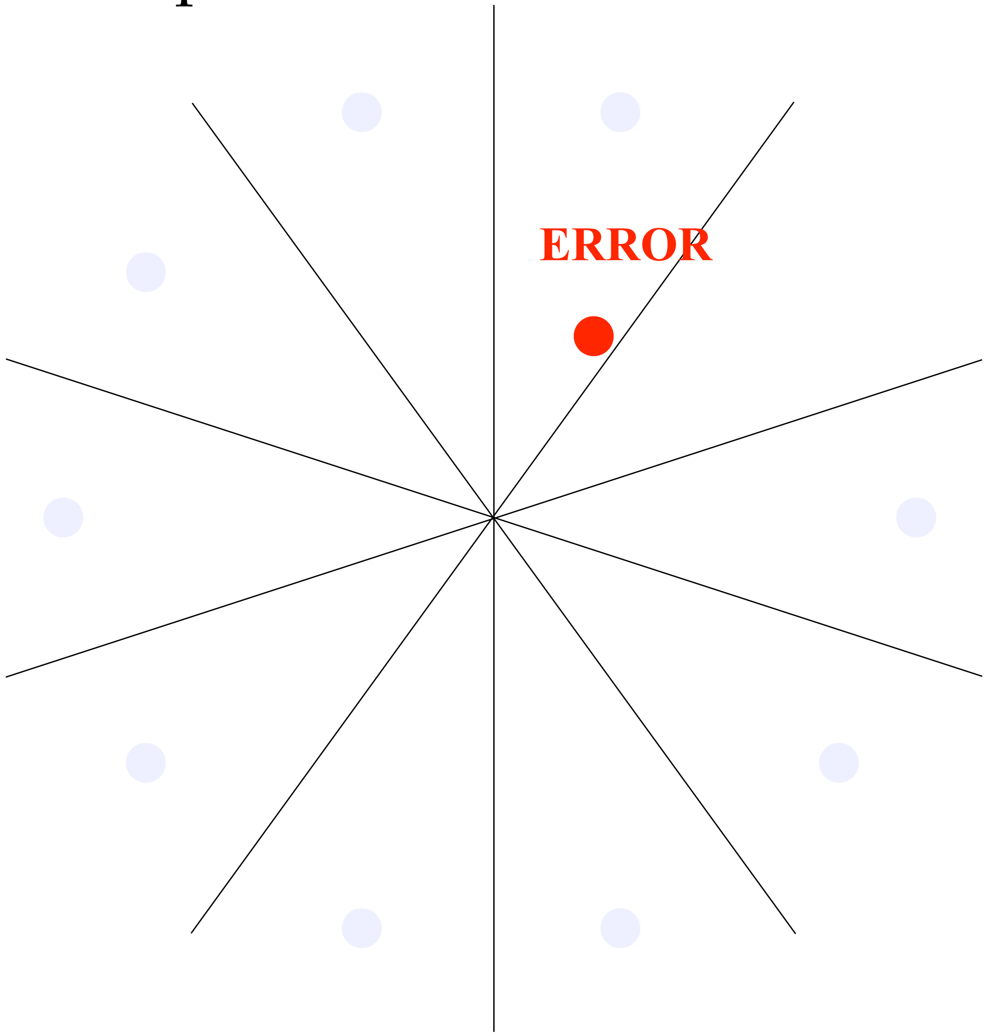
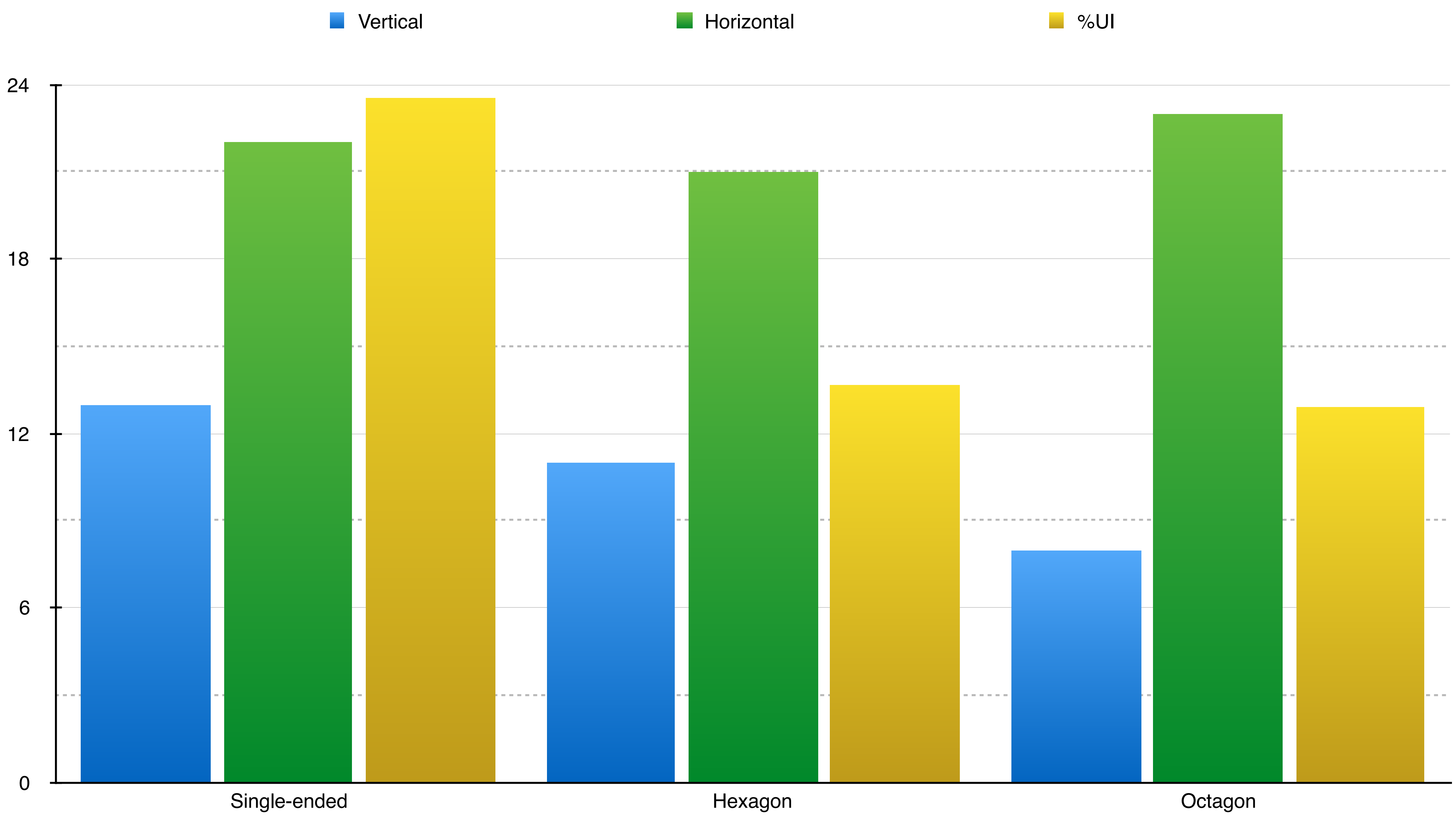
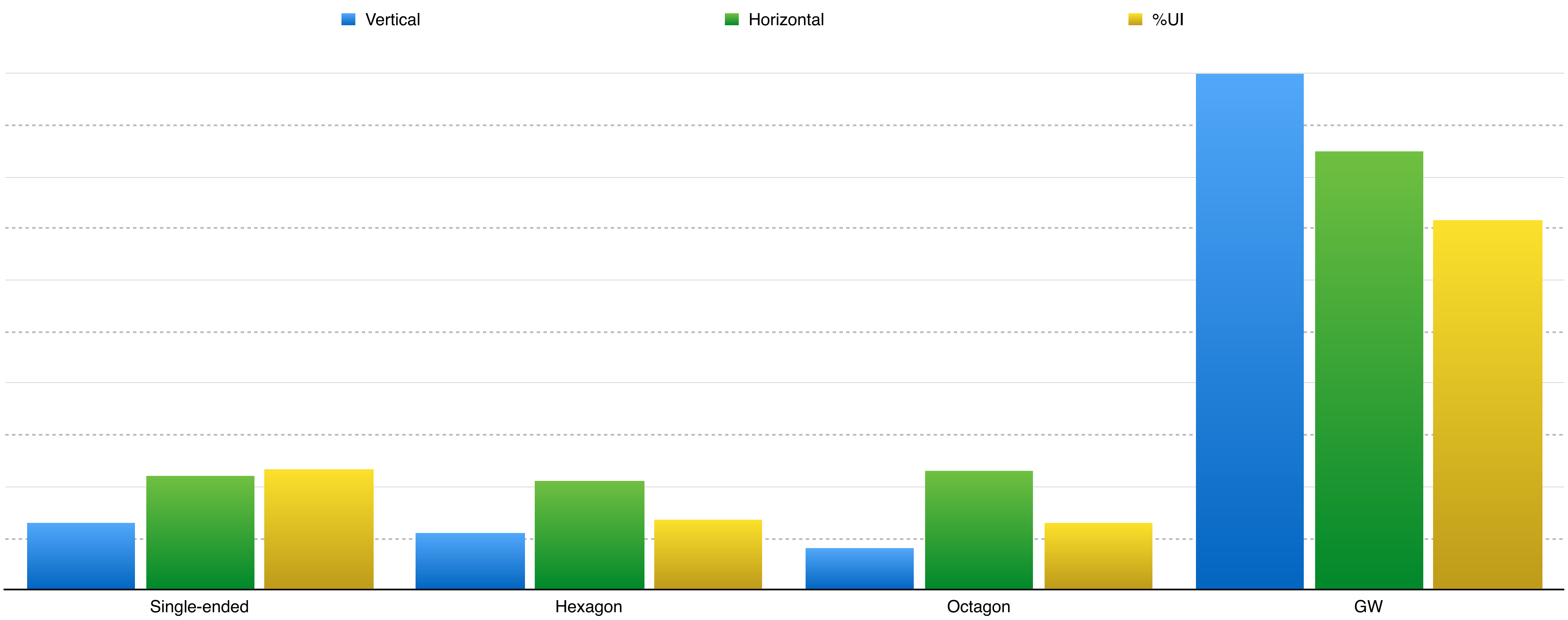


Increasing Immunity to Noise

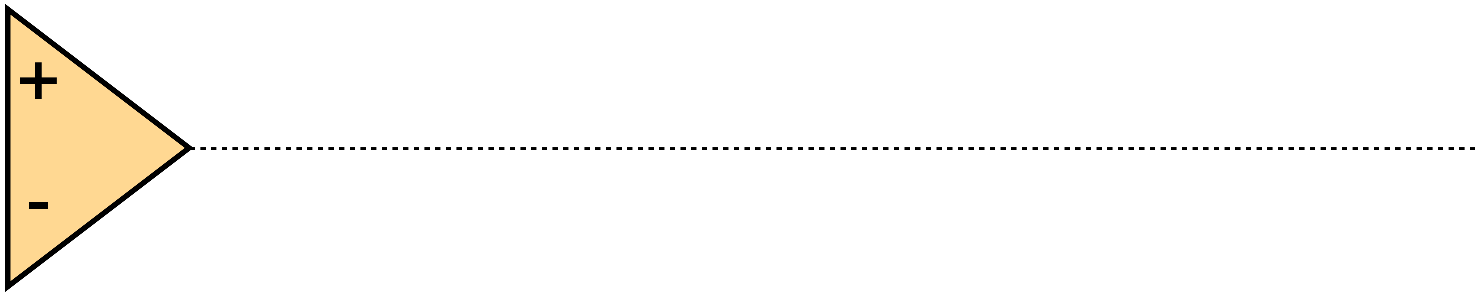


Increasing Immunity to Noise

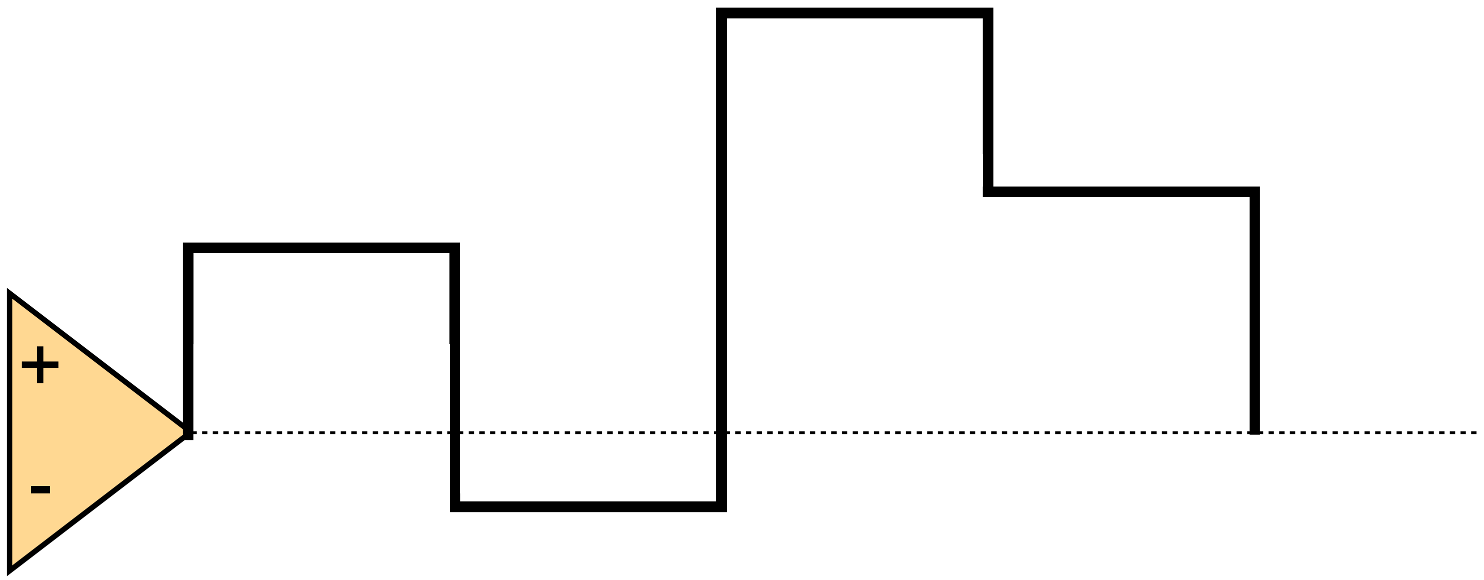


How was this designed?

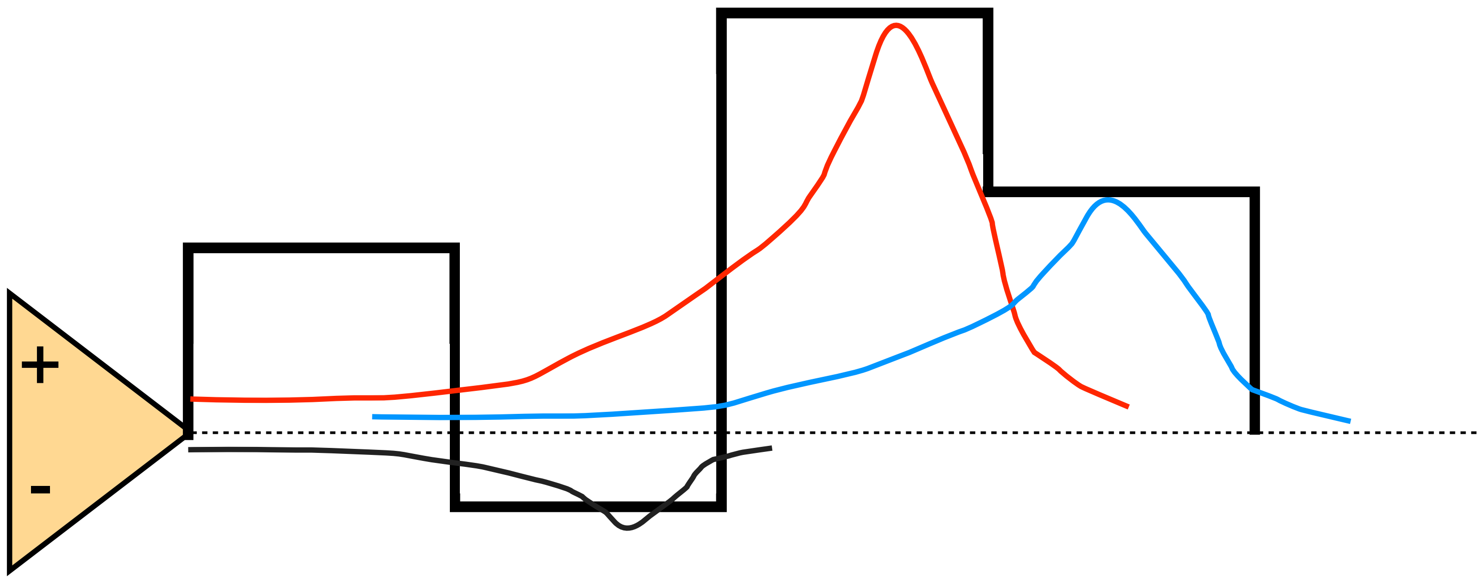
Intersymbol Interference Noise (ISI)



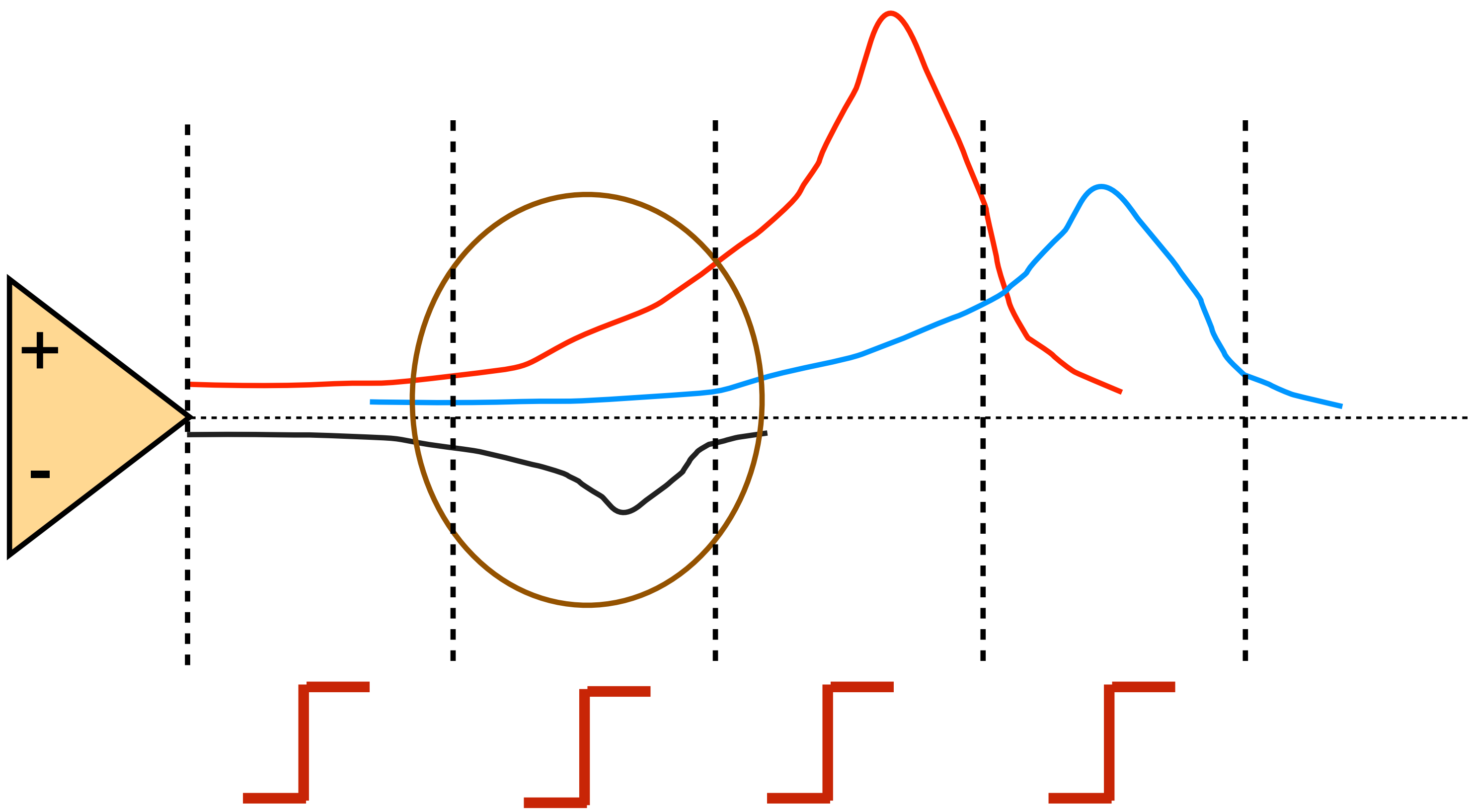
ISI



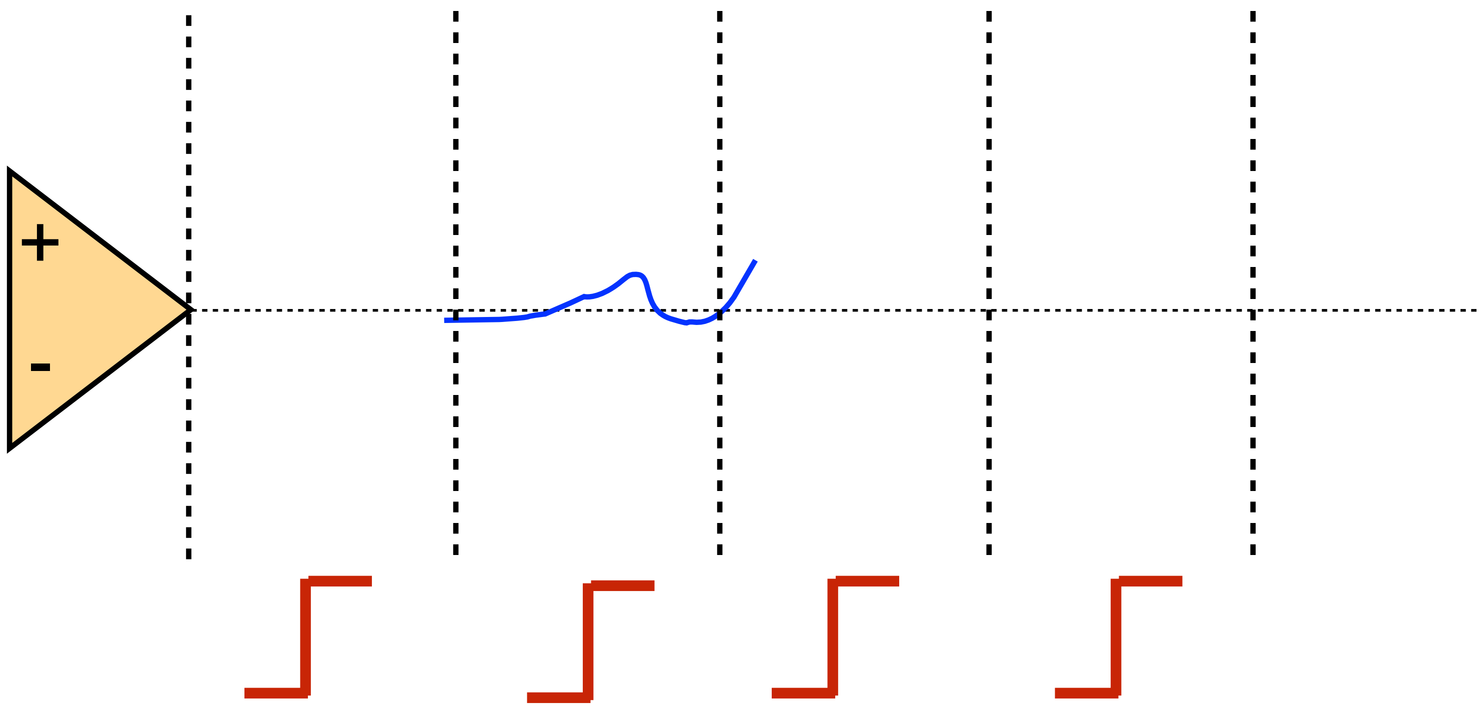
ISI



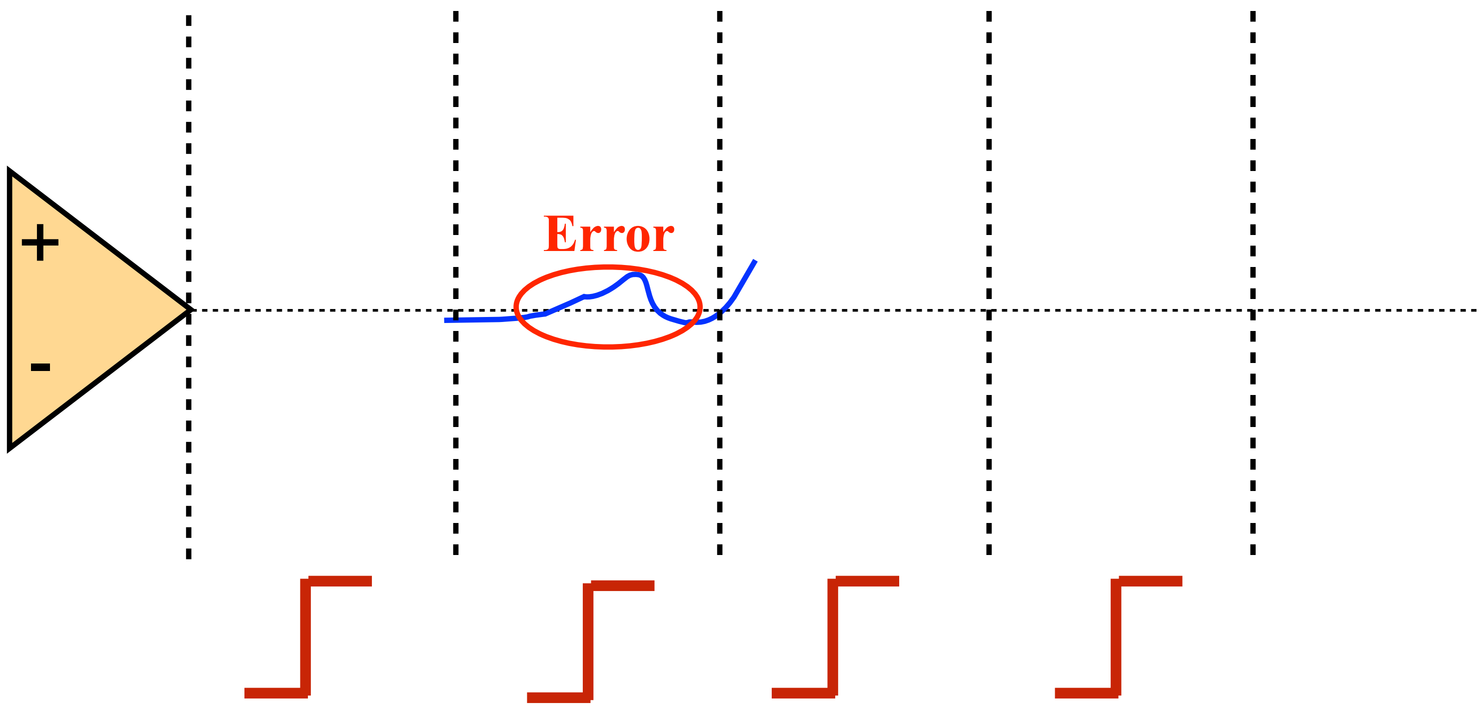
ISI



ISI

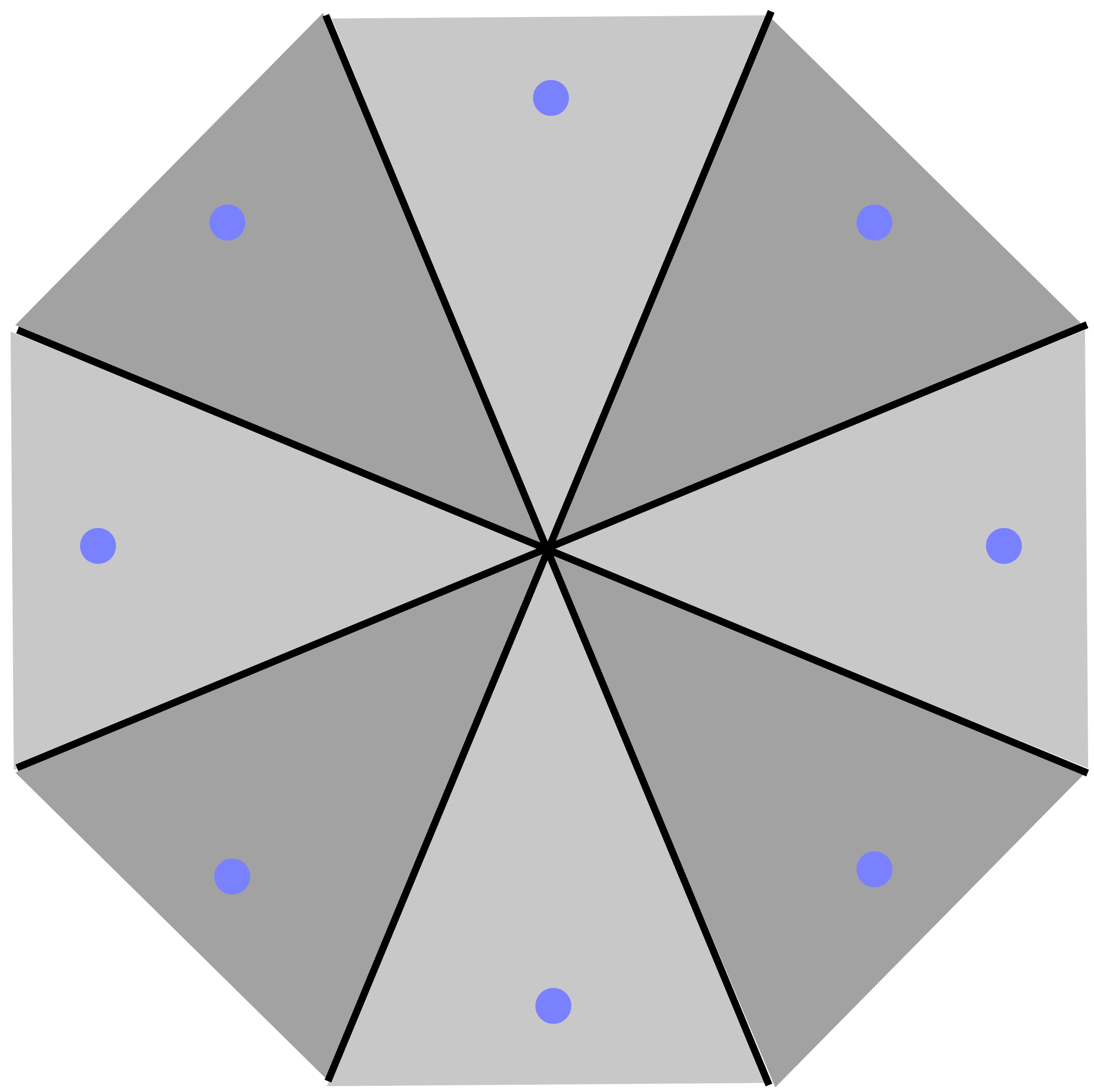


ISI

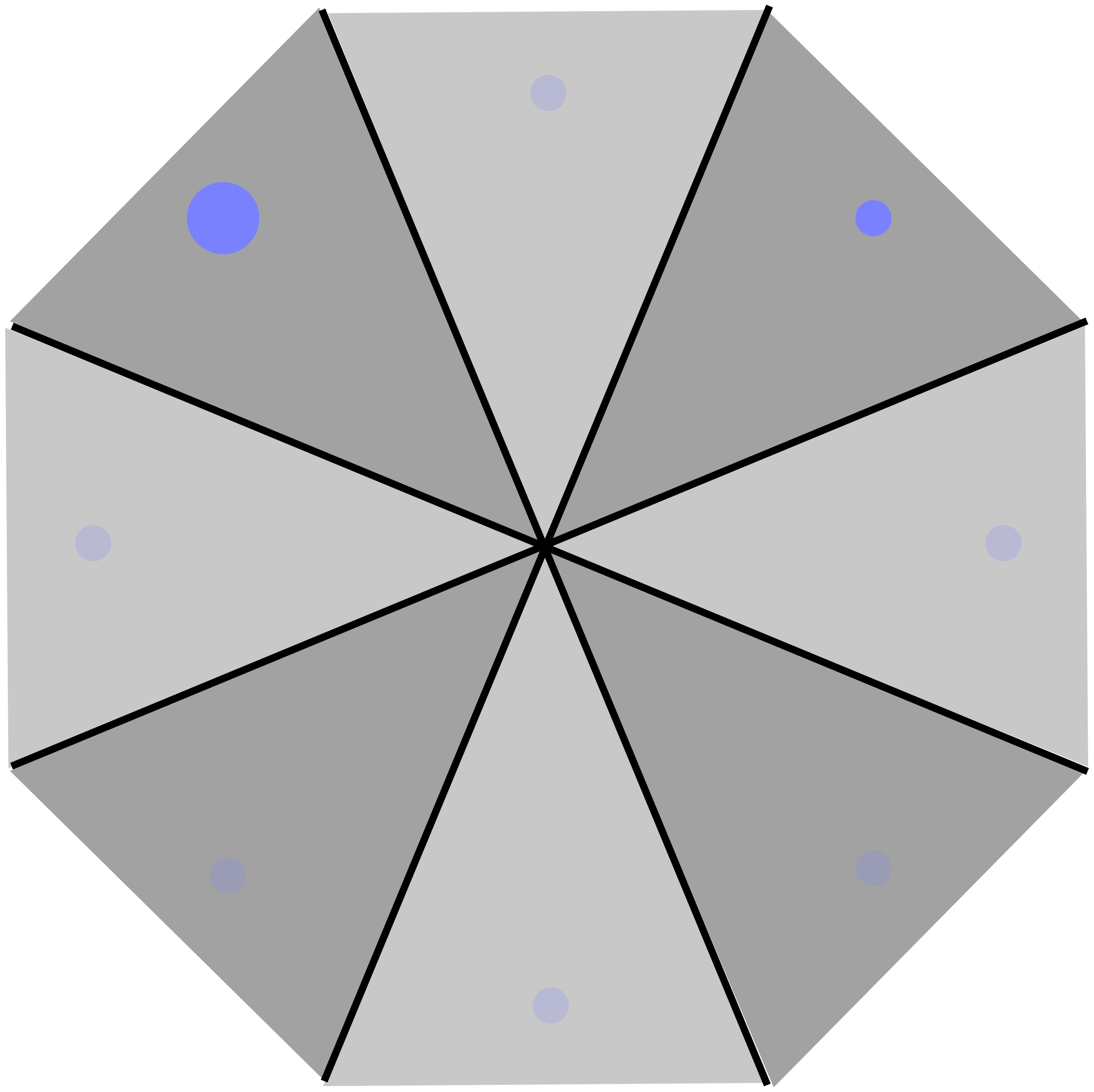


Leads to errors

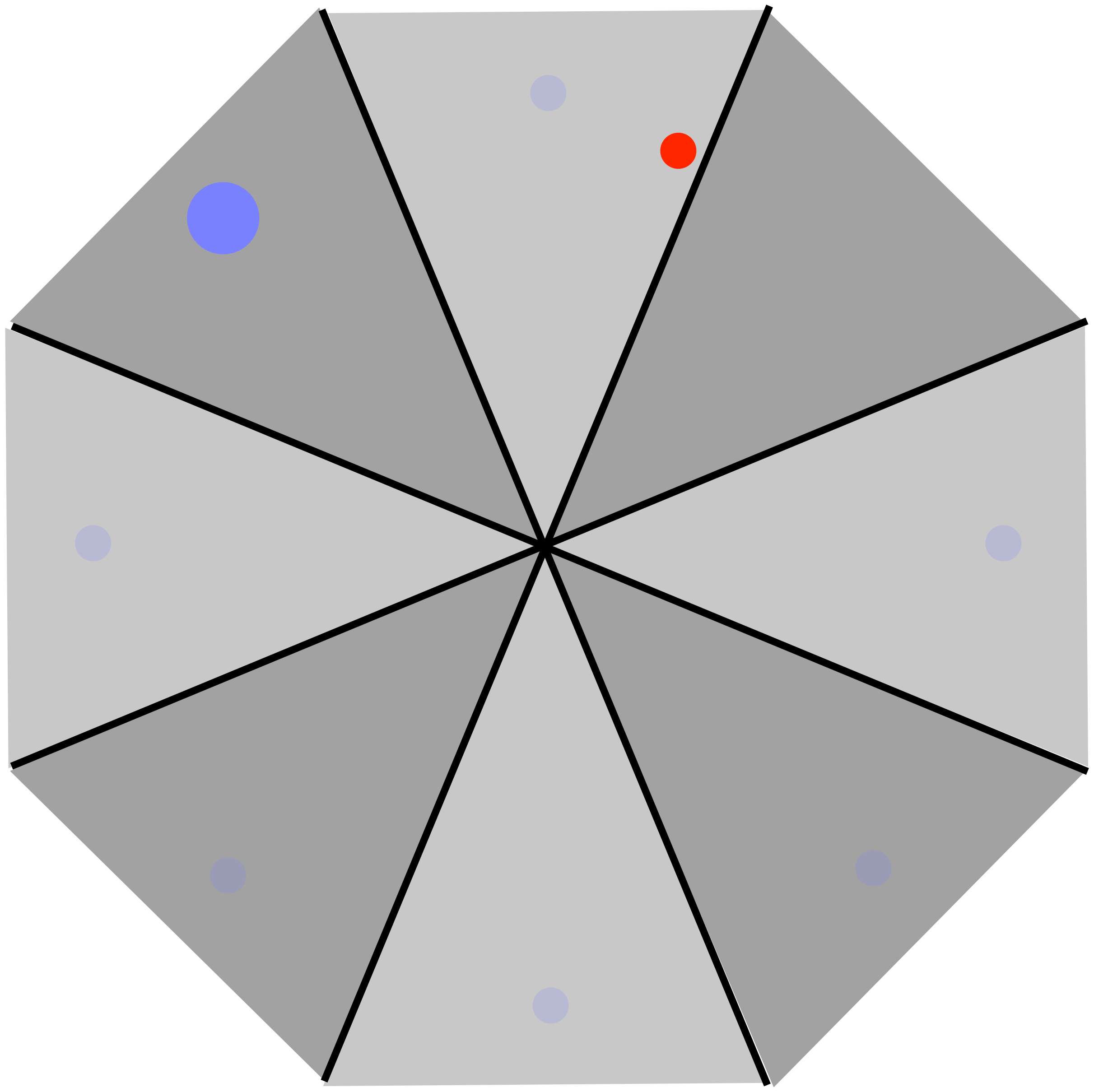
Geometric Interpretation



Geometric Interpretation

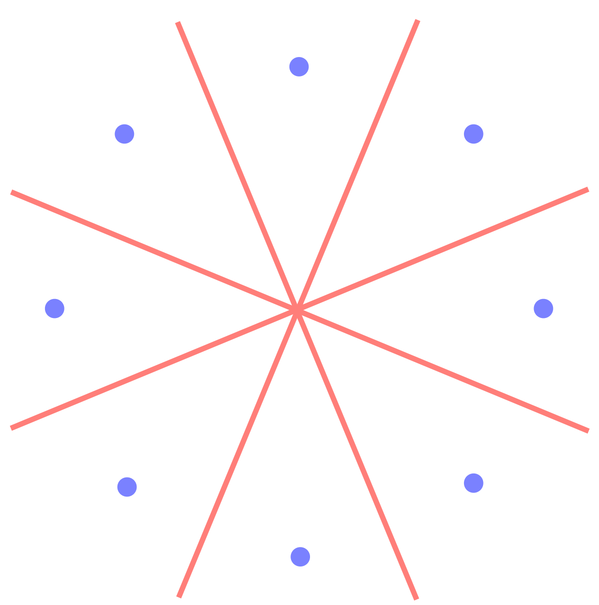


Geometric Interpretation



ISI-Ratio

- Figure of merit: a real number greater than or equal to 1.
- Ratio of furthest codeword from a hyperplane to the closest one.
- Maximum over all hyperplanes and all pairs of codewords



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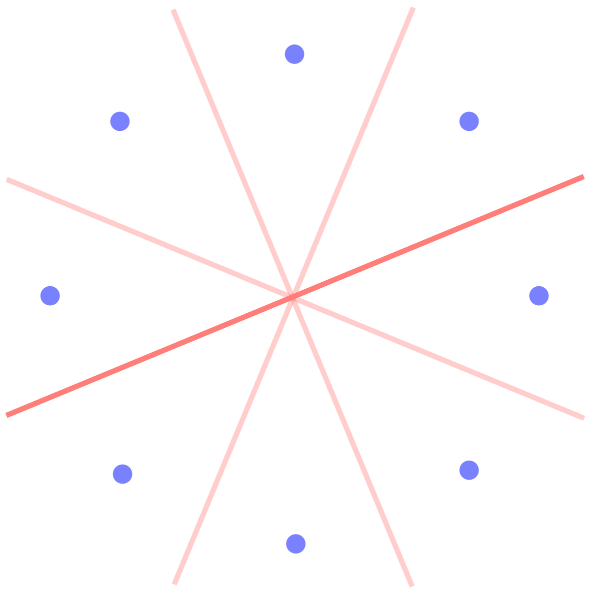

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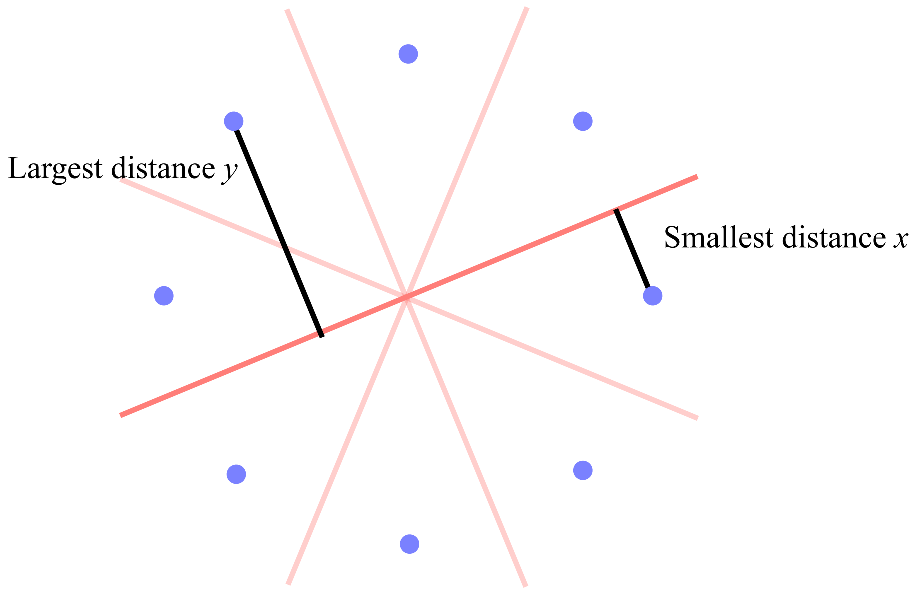
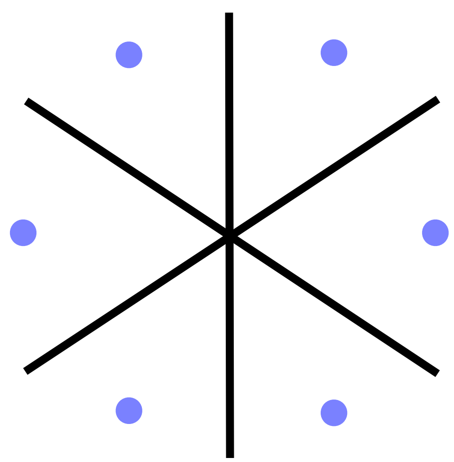
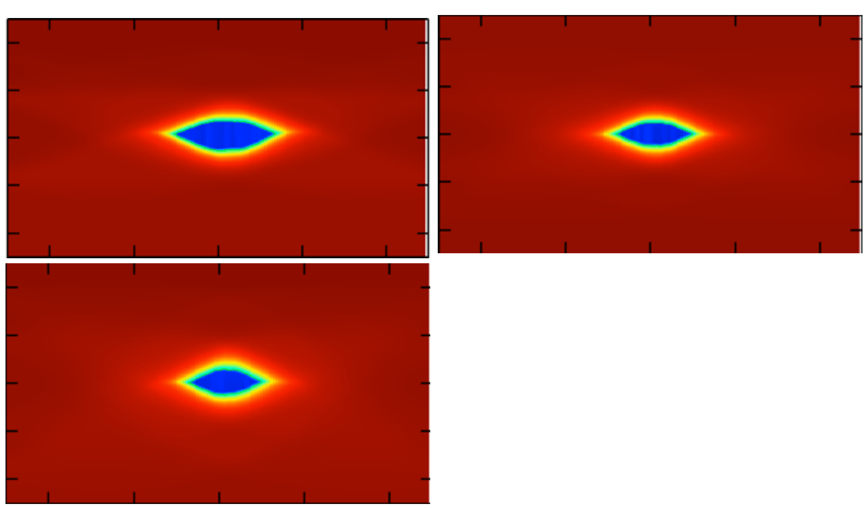


ISI ratio = y/x

Examples

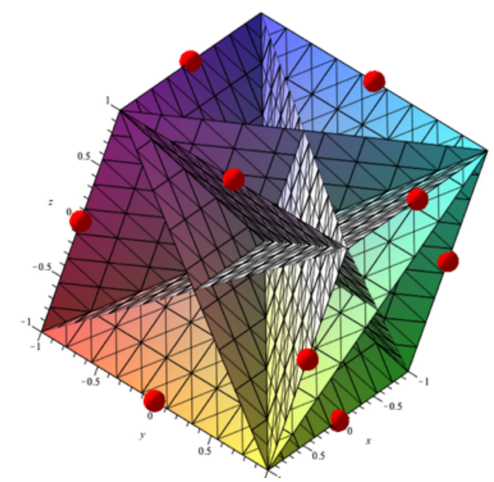


$I = 2$

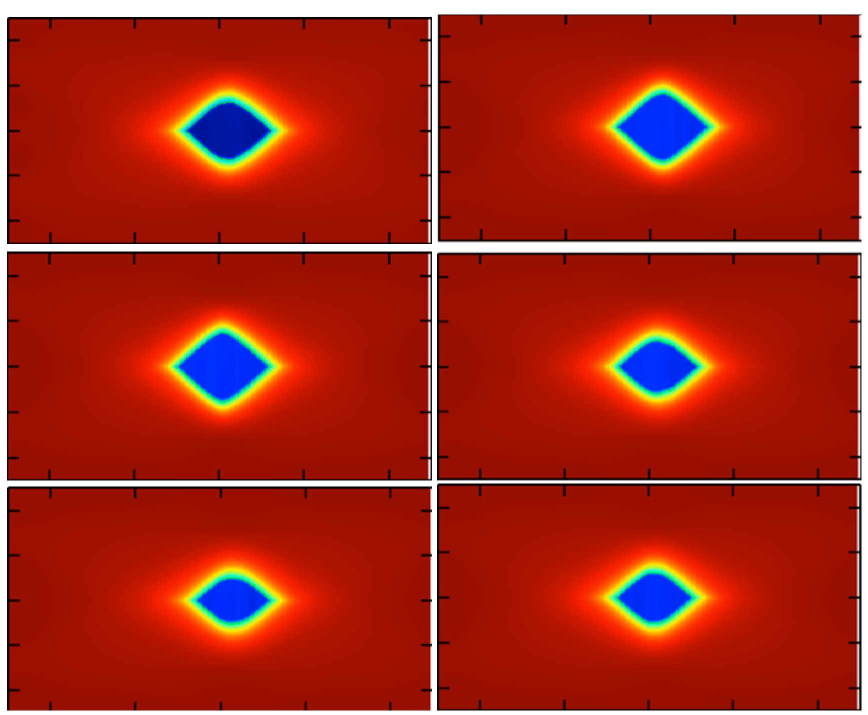


~ 17.5 - 24 psec

20 Gbps

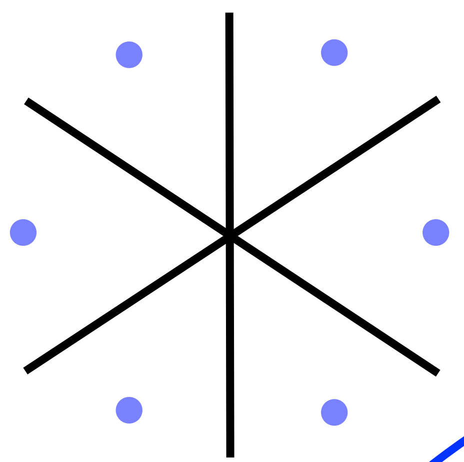


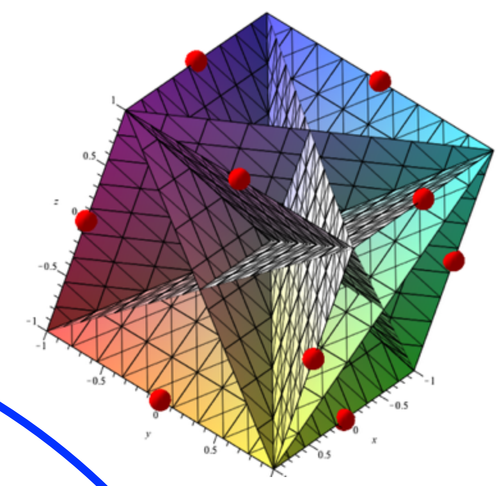
$I = 2$



~ 18 - 23 psec
18.7 Gbps

Examples

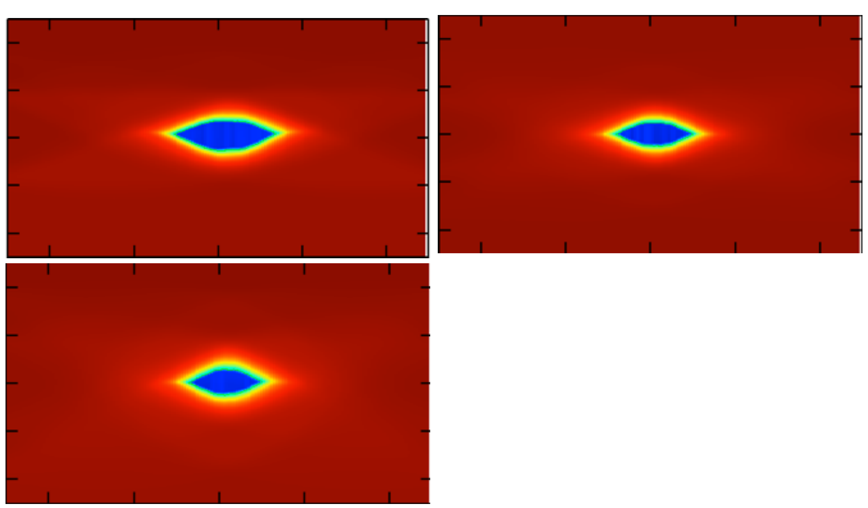




Same ISI ratio

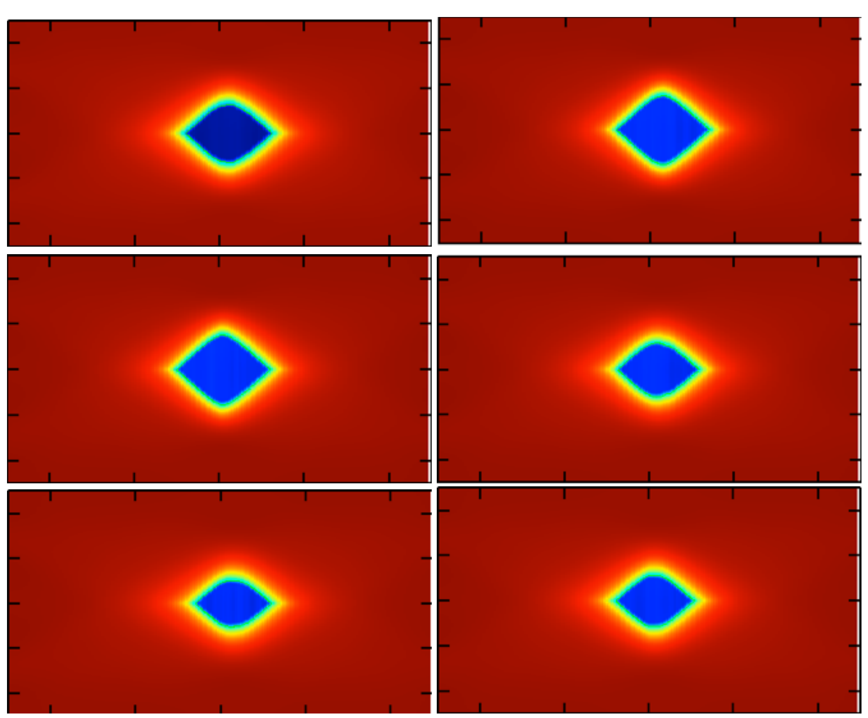
$I = 2$

$I = 2$



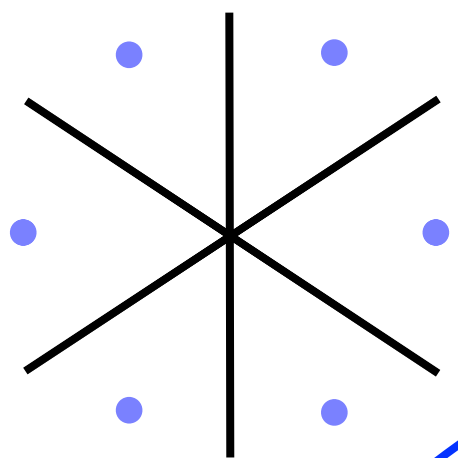
~ 17.5 - 24 psec

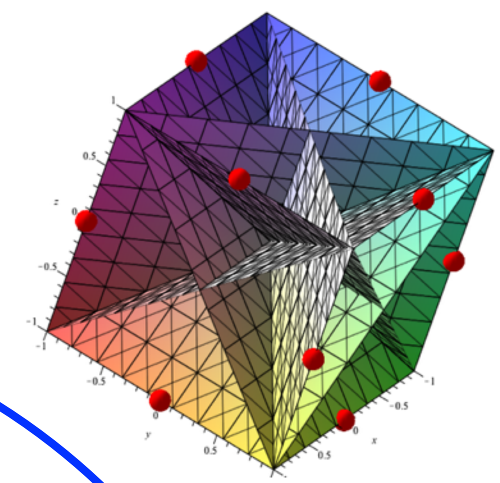
20 Gbps



~ 18 - 23 psec
18.7 Gbps

Examples

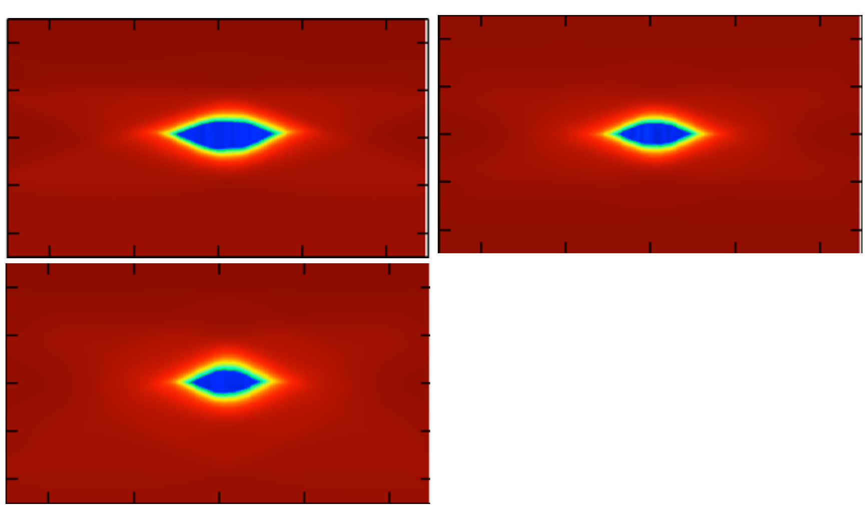




Same ISI ratio

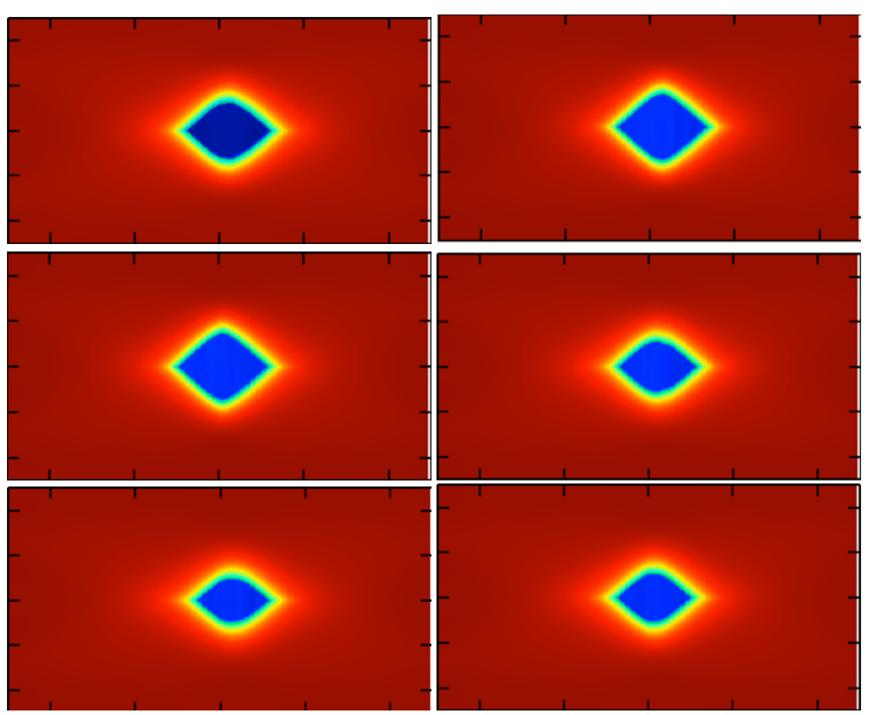
$I = 2$

$I = 2$



~ 17.5 - 24 psec

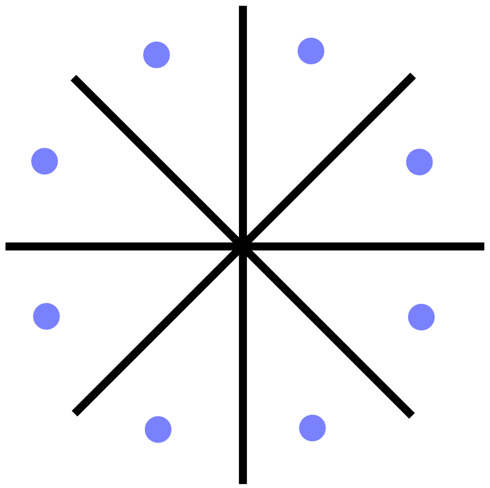
20 Gbps



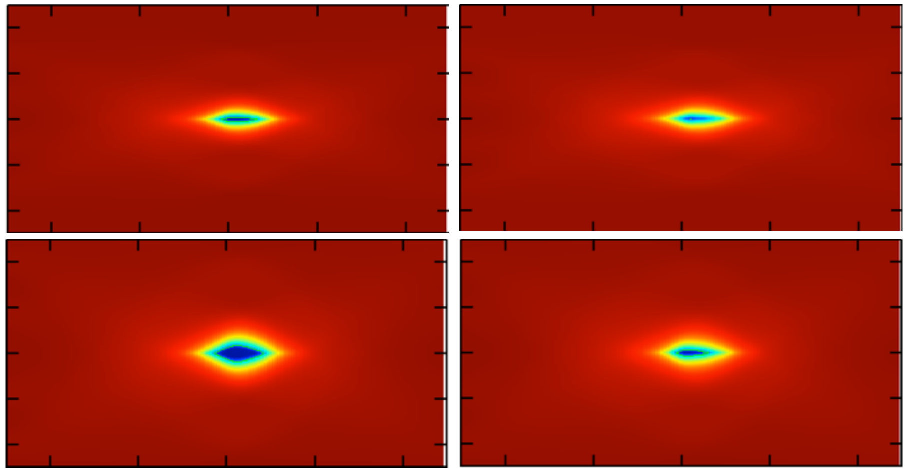
~ 18 - 23 psec
18.7 Gbps

Almost same width

Examples

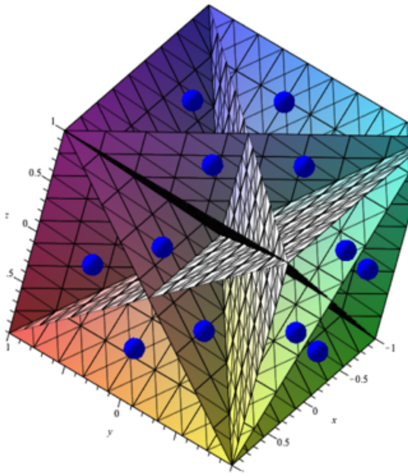


$$I = \sqrt{2} + 1$$

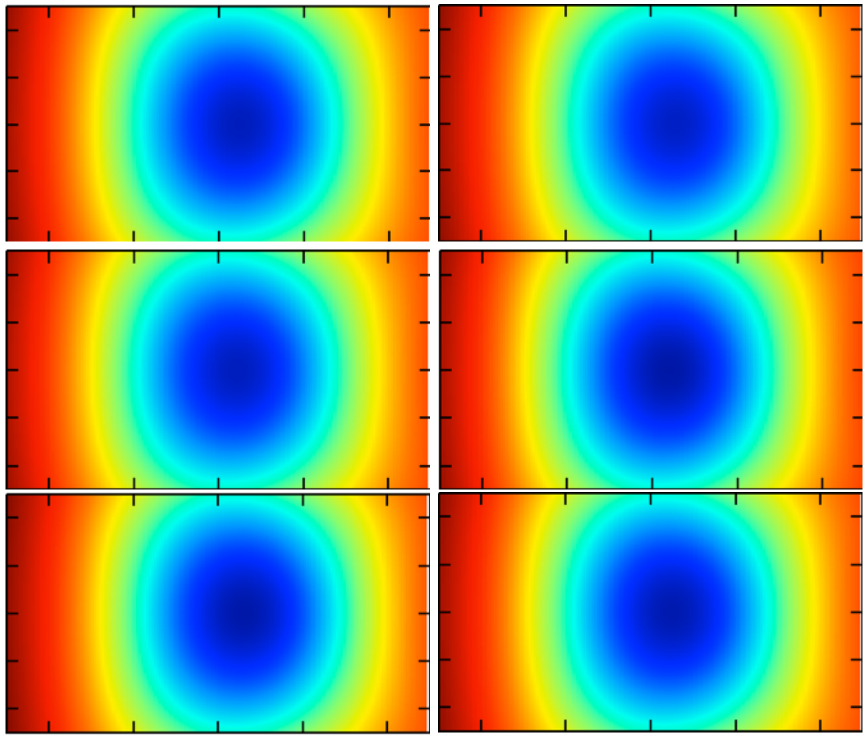


~ 7.5 - 12 psec

24 Gbps



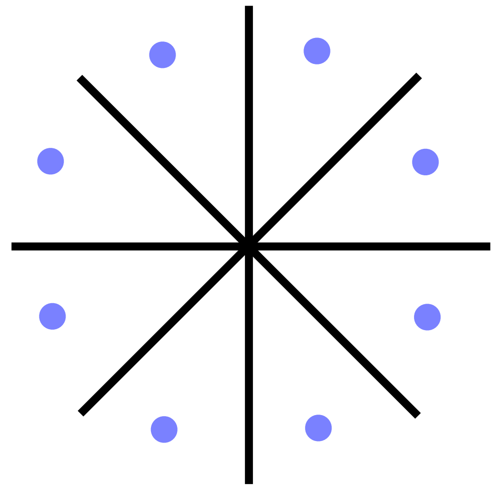
$$I = 3$$

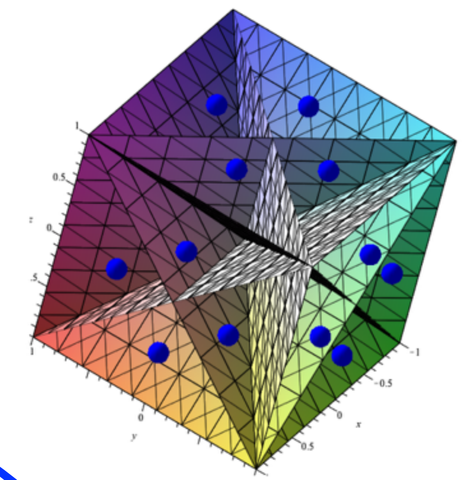


0 psec

24 Gbps

Examples

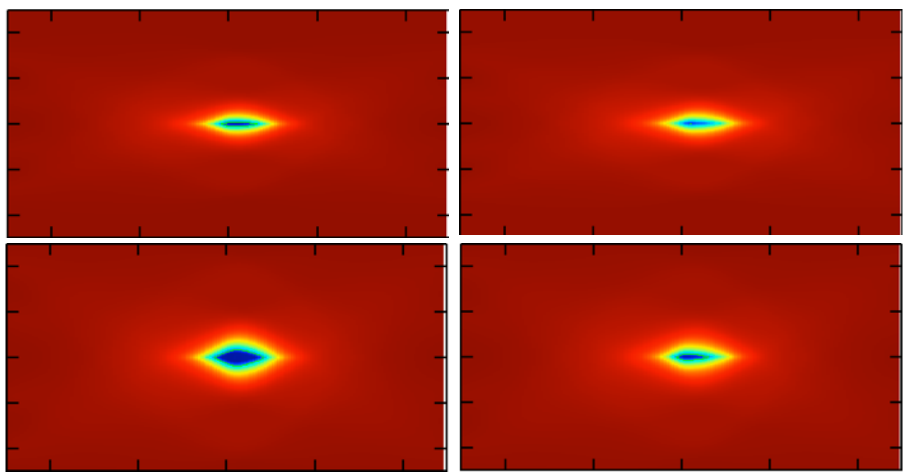




Higher ISI ratio loses....

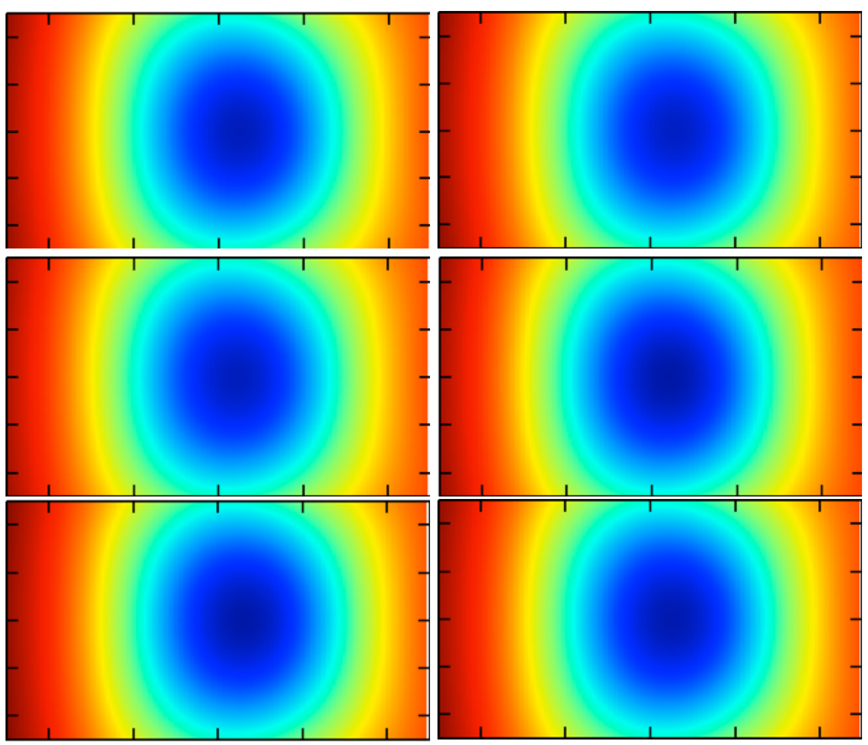
$$I = \sqrt{2} + 1$$

$$I = 3$$



~ 7.5 - 12 psec

24 Gbps



0 psec

24 Gbps

Noise

Noise

	Single-ended	Differential	4-PAM diff.	Chord Signaling (so far)
SSO	-	+	+/-	-
Ref	-	+	-	-
EMI	-	+	+	-
Common	-	+	+	-
ISI	+	-	- -	+/-
Conclusion	High speed problematic	Pin count problematic	High speed issues	May have issues

Noise

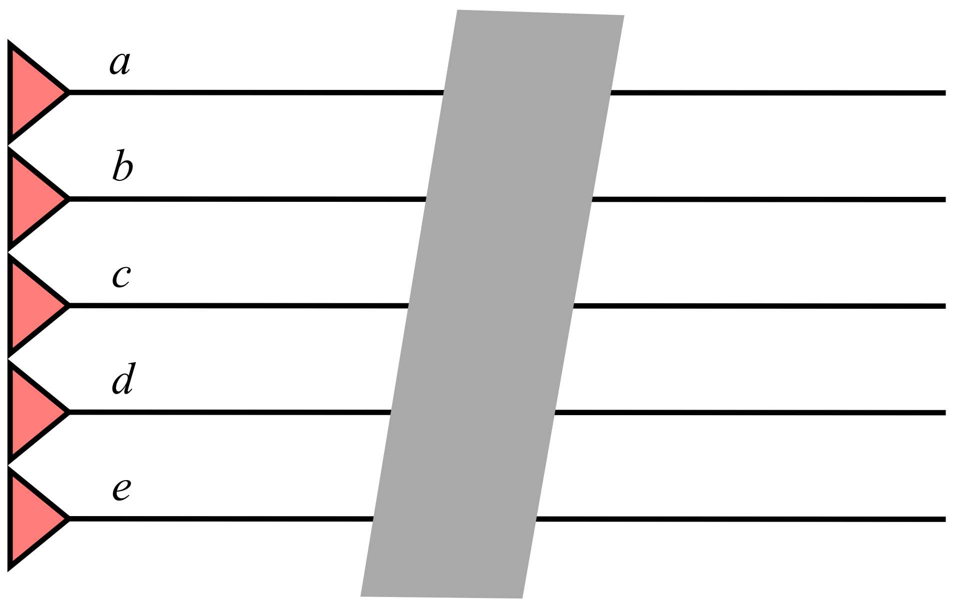
	Single-ended	Differential	4-PAM diff.	Chord Signaling (so far)
SSO	-	+	+/-	-
Ref	-	+	-	-
EMI	-	+	+	-
Common	-	+	+	-
ISI	+	-	- -	+ by design
Conclusion	High speed problematic	Pin count problematic	High speed issues	May have issues

Reference, EMI, Common Mode Noise and SSO

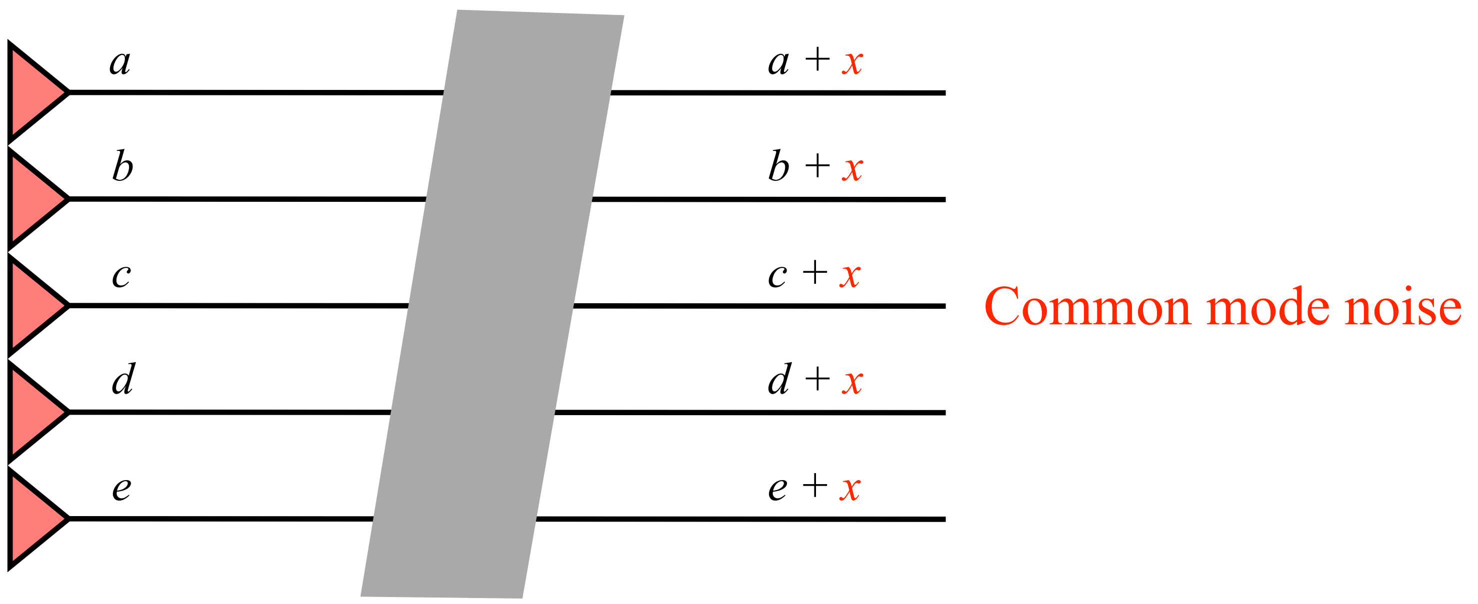
Noise Mitigation

Common Mode noise, EMI noise, SSO, and reference noise can be dealt with one elegant construction.

Common Mode Noise



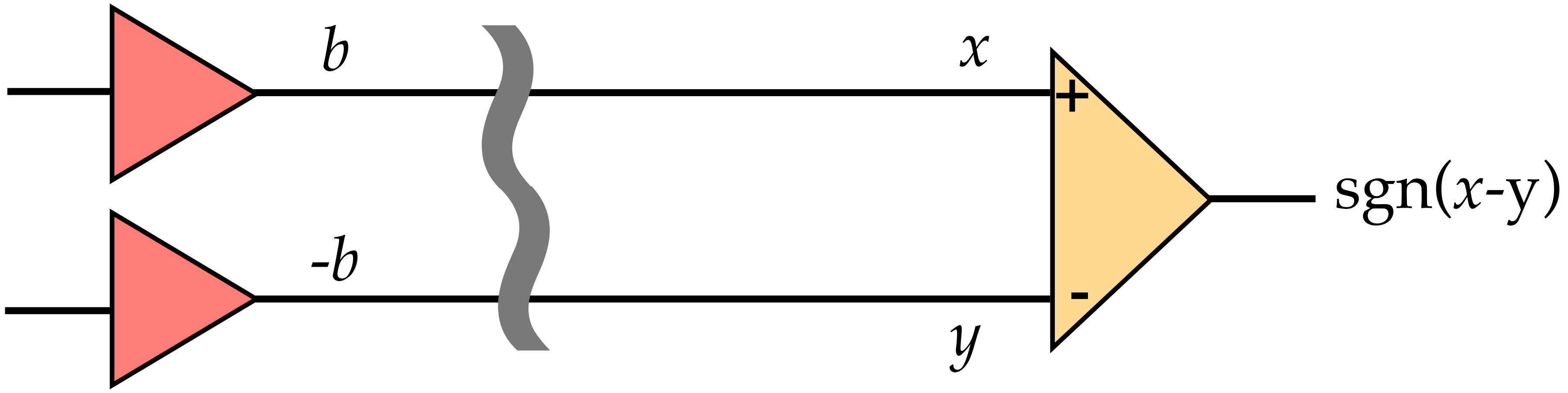
Common Mode Noise



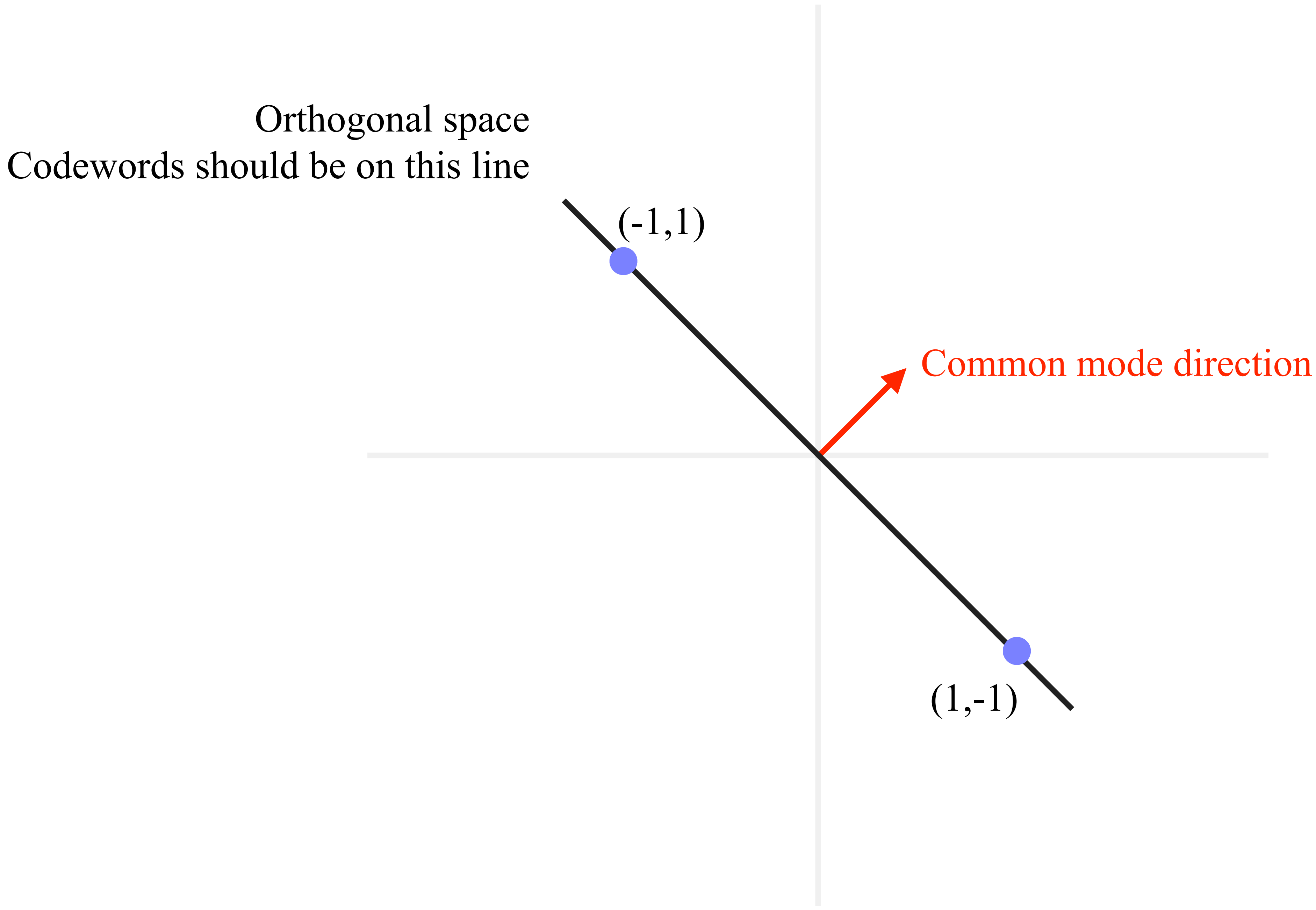
- Bad for signal integrity
- Common mode should be rejected at receiver
  - Means that comparators should evaluate to 0 on vector (1,1,1,...,1)
- Codewords should have no common mode component
  - Common mode component is along vector (1,1,1,...,1)
  - Means that the sum of the values on the wires should be constant.

KANDOU BUS

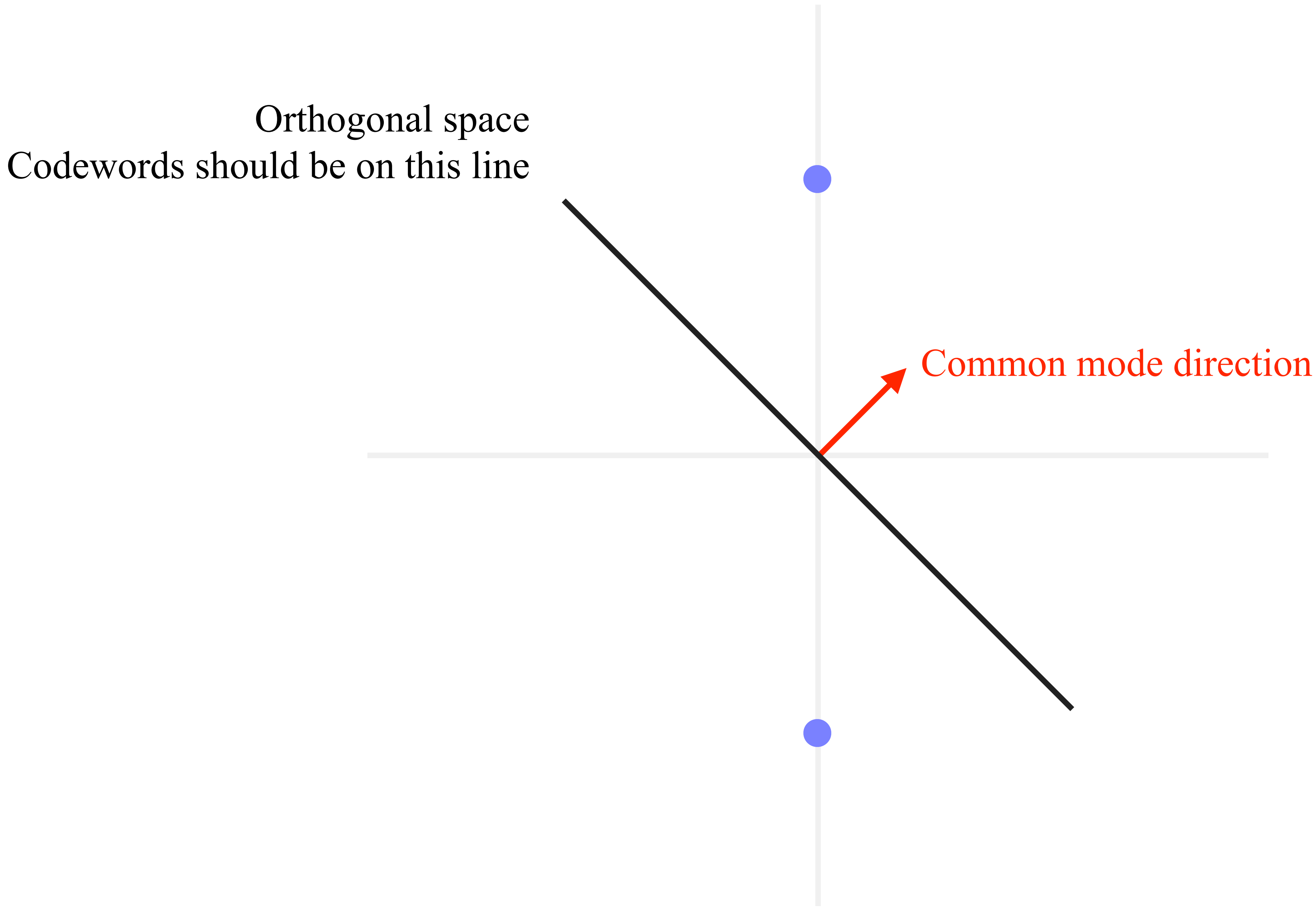
CM Resistance Differential Signaling



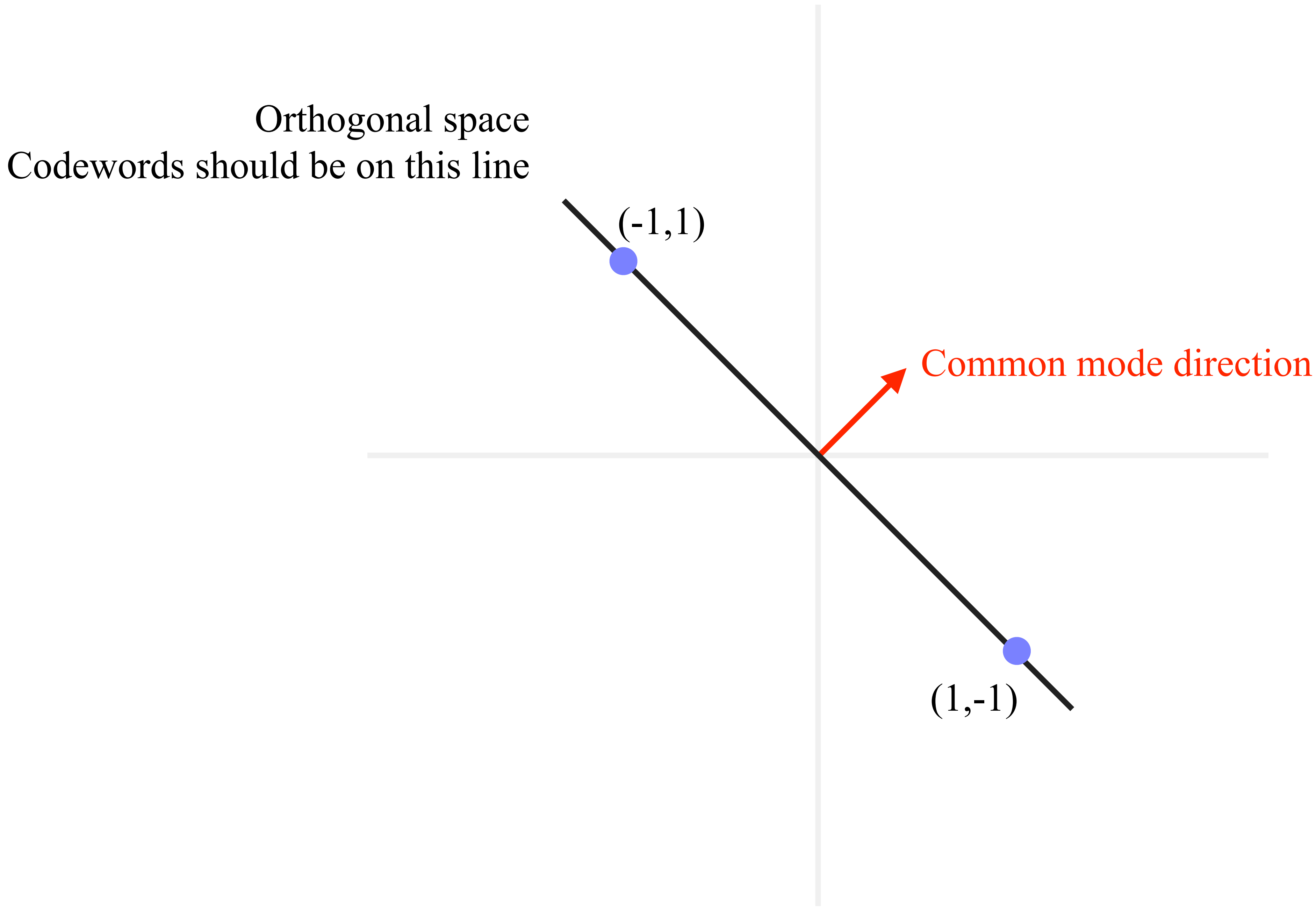
CM Resistant Codes
Differential Signaling



Differential from Single Ended



Differential from Single Ended



Orthogonal Transformation

Tempering Process

- Creates CM resistant Chordal code from any Chordal code
- The number of wires of the interface grows by one
- All other parameters of the code stay the same (including the ISI ratio)

- Use Tempering Orthogonal Transformation on the codewords.

Tempering Process

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- Use Tempering Orthogonal Transformation on the codewords.

$$\begin{matrix} * & * & * & * & * & * \\ * & * & * & * & * & * \\ * & * & * & * & * & * \\ * & * & * & * & * & * \\ * & * & * & * & * & * \\ * & * & * & * & * & * \end{matrix}$$

Orthogonal matrix

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- Creates CM resistant Chordal code from any Chordal code
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- Use Tempering Orthogonal Transformation on the codewords.

$$\begin{matrix} * \\ * \\ * \\ * \\ * \\ * \end{matrix} + \begin{matrix} * \\ * \\ * \\ * \\ * \\ * \end{matrix} + \begin{matrix} * \\ * \\ * \\ * \\ * \\ * \end{matrix} + \begin{matrix} * \\ * \\ * \\ * \\ * \\ * \end{matrix} + \begin{matrix} * \\ * \\ * \\ * \\ * \\ * \end{matrix} + \begin{matrix} * \\ * \\ * \\ * \\ * \\ * \end{matrix} = \begin{matrix} * \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{matrix}$$

Tempering orthogonal matrix

Tempering Process

- Creates CM resistant Chordal code from any Chordal code
- The number of wires of the interface grows by one
- All other parameters of the code stay the same (including the ISI ratio)

- Use Tempering Orthogonal Transformation on the codewords.

$$\begin{pmatrix} * \\ * \\ * \\ * \\ * \\ * \end{pmatrix} + \begin{pmatrix} * \\ * \\ * \\ * \\ * \\ * \end{pmatrix} + \begin{pmatrix} * \\ * \\ * \\ * \\ * \\ * \end{pmatrix} + \begin{pmatrix} * \\ * \\ * \\ * \\ * \\ * \end{pmatrix} + \begin{pmatrix} * \\ * \\ * \\ * \\ * \\ * \end{pmatrix} + \begin{pmatrix} * \\ * \\ * \\ * \\ * \\ * \end{pmatrix} = \begin{pmatrix} * \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix}$$

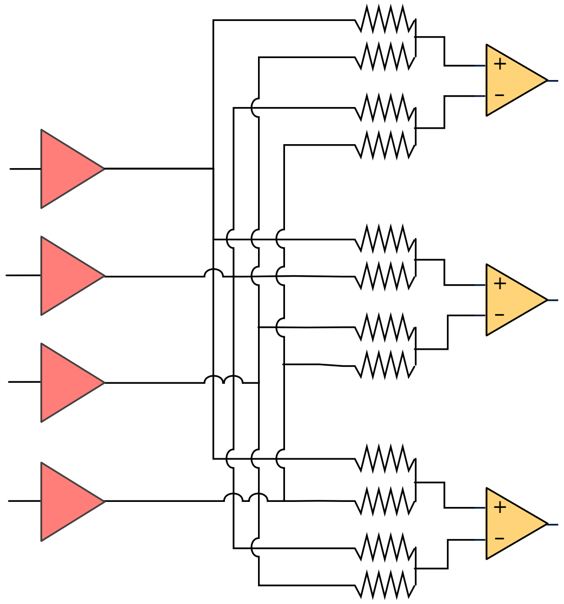
Tempering orthogonal matrix

- (0 | old codeword) * Tempering Orthogonal Matrix = new codeword
- (0 | old comparator) * Tempering Orthogonal Matrix = new comparator

Examples
ENRZ

$$\frac{1}{2}\begin{pmatrix} 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \end{pmatrix}$$

Hadamard Transform



ACTUAL IMPLEMENTATION
MAY BE DIFFERENT

$$\pm(1, -1/3, -1/3, -1/3)$$
$$\pm(-1/3, 1, -1/3, -1/3)$$
$$\pm(-1/3, -1/3, 1, -1/3)$$
$$\pm(-1/3, -1/3, -1/3, 1)$$

3/4

Common Mode Noise

	Single-ended	Differential	4-PAM diff.	Chord Signaling (so far)
SSO	-	+	+/-	-
Ref	-	+	-	-
EMI	-	+	+	-
Common	-	+	+	-
ISI	+	-	- -	+
Conclusion	High speed problematic	Pin count problematic	High speed issues	May have issues

Common Mode Noise

Disappears by construction.

	Single-ended	Differential	4-PAM diff.	Chord Signaling (so far)
SSO	-	+	+/-	-
Ref	-	+	-	-
EMI	-	+	+	-
Common	-	+	+	+
ISI	+	-	- -	+
Conclusion	High speed problematic	Pin count problematic	High speed issues	May have issues

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Reference Noise

	Single-ended	Differential	4-PAM diff.	Chord Signaling (so far)
SSO	-	+	+/-	-
Ref	-	+	-	-
EMI	-	+	+	-
Common	-	+	+	+
ISI	+	-	- -	+
Conclusion	High speed problematic	Pin count problematic	High speed issues	May have issues

Reference Noise

Disappears, since no reference needed.

	Single-ended	Differential	4-PAM diff.	Chord Signaling (so far)
SSO	-	+	+/-	-
Ref	-	+	-	+
EMI	-	+	+	-
Common	-	+	+	+
ISI	+	-	- -	+
Conclusion	High speed problematic	Pin count problematic	High speed issues	May have issues

EMI Noise

	Single-ended	Differential	4-PAM diff.	Chord Signaling (so far)
SSO	-	+	+/-	-
Ref	-	+	-	+
EMI	-	+	+	-
Common	-	+	+	+
ISI	+	-	- -	+
Conclusion	High speed problematic	Pin count problematic	High speed issues	May have issues

EMI Noise

Largely mitigated, since sum of currents on the wires is 0 (far-fields cancel each other). Separate theory developed.

	Single-ended	Differential	4-PAM diff.	Chord Signaling (so far)
SSO	-	+	+/-	-
Ref	-	+	-	+
EMI	-	+	+	+
Common	-	+	+	+
ISI	+	-	- -	+
Conclusion	High speed problematic	Pin count problematic	High speed issues	May have issues

SSO Noise

Largely mitigated through additional constraint on tempering matrix.

	Single-ended	Differential	4-PAM diff.	Chord Signaling
SSO	-	+	+/-	+
Ref	-	+	-	+
EMI	-	+	+	+
Common	-	+	+	+
ISI	+	-	- -	+
Conclusion	High speed problematic	Pin count problematic	High speed issues	

Chord Signaling

	Chord Signaling
SSO	+
Ref	+
EMI	+
Common	+
ISI	+
Conclusion	Can be used in a wide range of applications

Definition

A (n, N, c, I)-*Chordal Code* (CC) is a pair (C, Λ) where

- C is a subset of $[-1,1]^n$ of size N (set of codewords)
- Λ is a subset of $(\mathbb{R}^n)^*$ of size c (set of comparators)

such that

- (Distinguishability) $\forall c_1, c_2 \in C, c_1 \neq c_2 \exists \lambda \in \Lambda \colon \lambda(c_1)\lambda(c_2) < 0$
- (ISI-tolerance) $\forall \lambda \in \Lambda, c_1, c_2 \in C \colon \dfrac{|\lambda(c_1)|}{|\lambda(c_2)|} \leq I$

Lots of practical concerns swept under the rug.

Given n and N, find minimum I, such that there exists a (n, N, c, I)-CC for some c.

Example of a Concrete Question

What is the best ISI-ratio for $n = 3$, $N = 16$?

Best result so far: 2.39304, 11 comparators,
not practical

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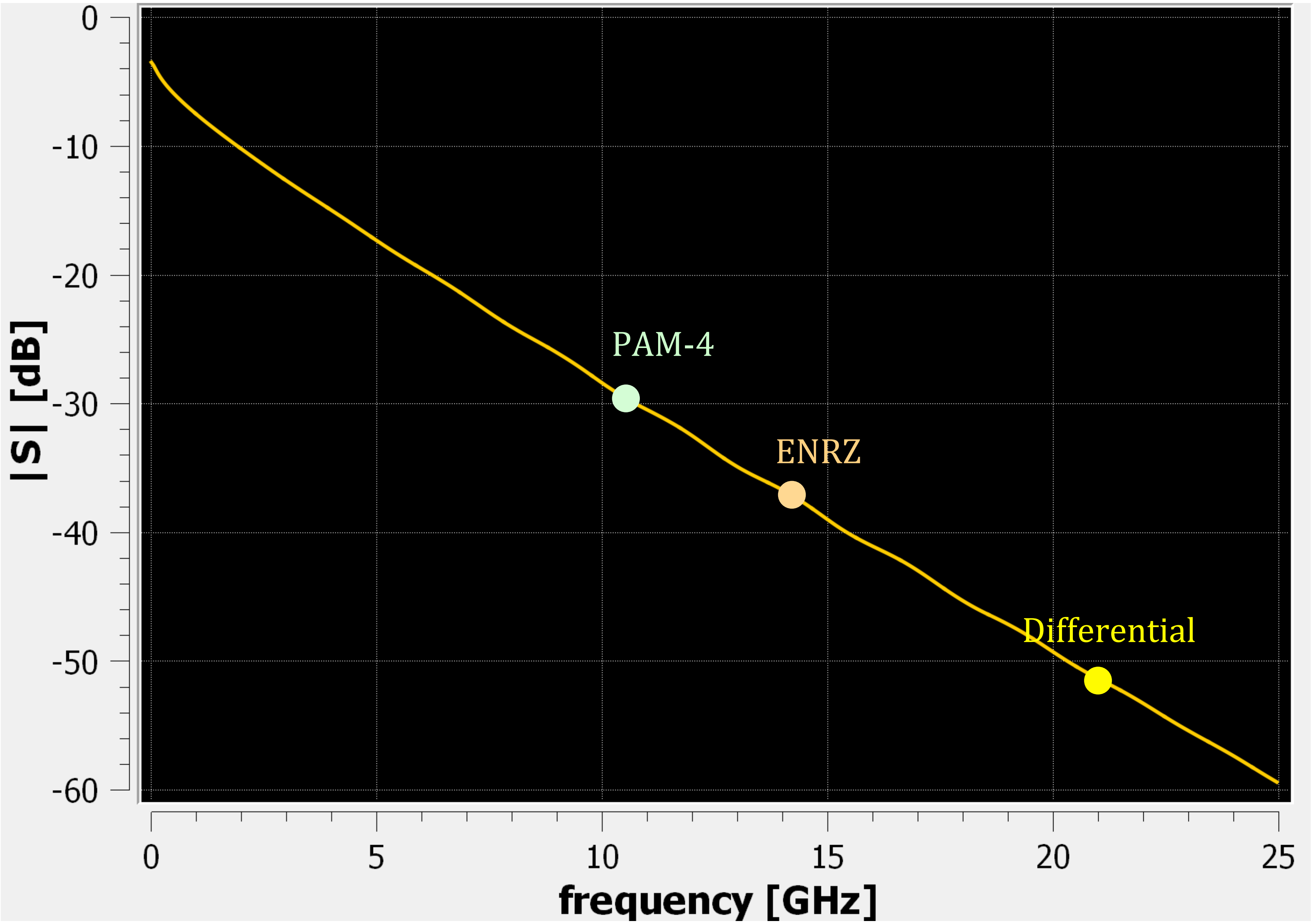
But....

Theory of these codes is subject of a more technical talk

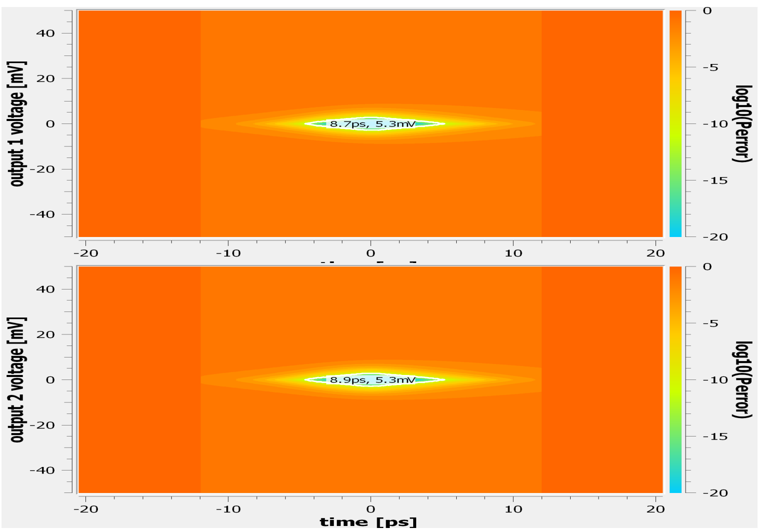
Example



0
-10
-20
-30
-40
-50
-60
|S| [dB]
PAM-4
ENRZ
Differential
0
5
10
15
20
25
frequency [GHz]

Example

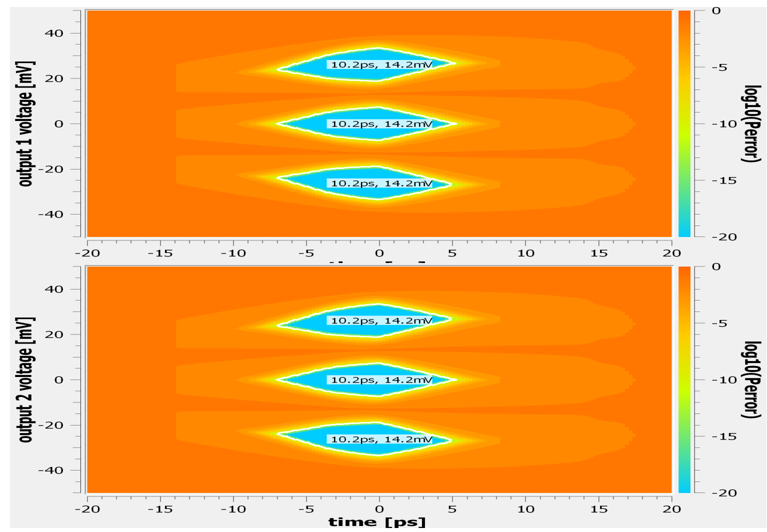
Differential



	Horizontal opening	Vertical opening
Eye 1	8.7 psec	5.3 mV
Eye 2	8.9 psec	5.3 mV

ISI-ratio = 1
21 GHz clock

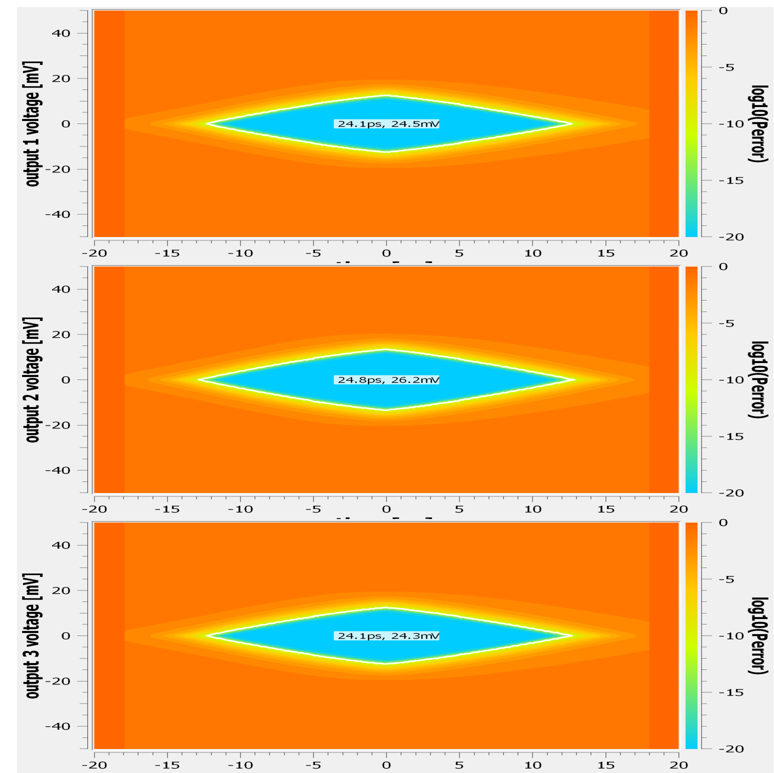
Differential PAM-4



	Horizontal opening	Vertical opening
Eyes 1-6	10.2 psec	14.2 mV

ISI-ratio = 3
10.5 GHz clock

ENRZ



	Horizontal opening	Vertical opening
Eye 1	24.1 psec	24.5 mV
Eye 2	24.8 psec	26.2 mV
Eye 3	24.1 psec	24.3 mV

ISI-ratio = 1
14 GHz clock

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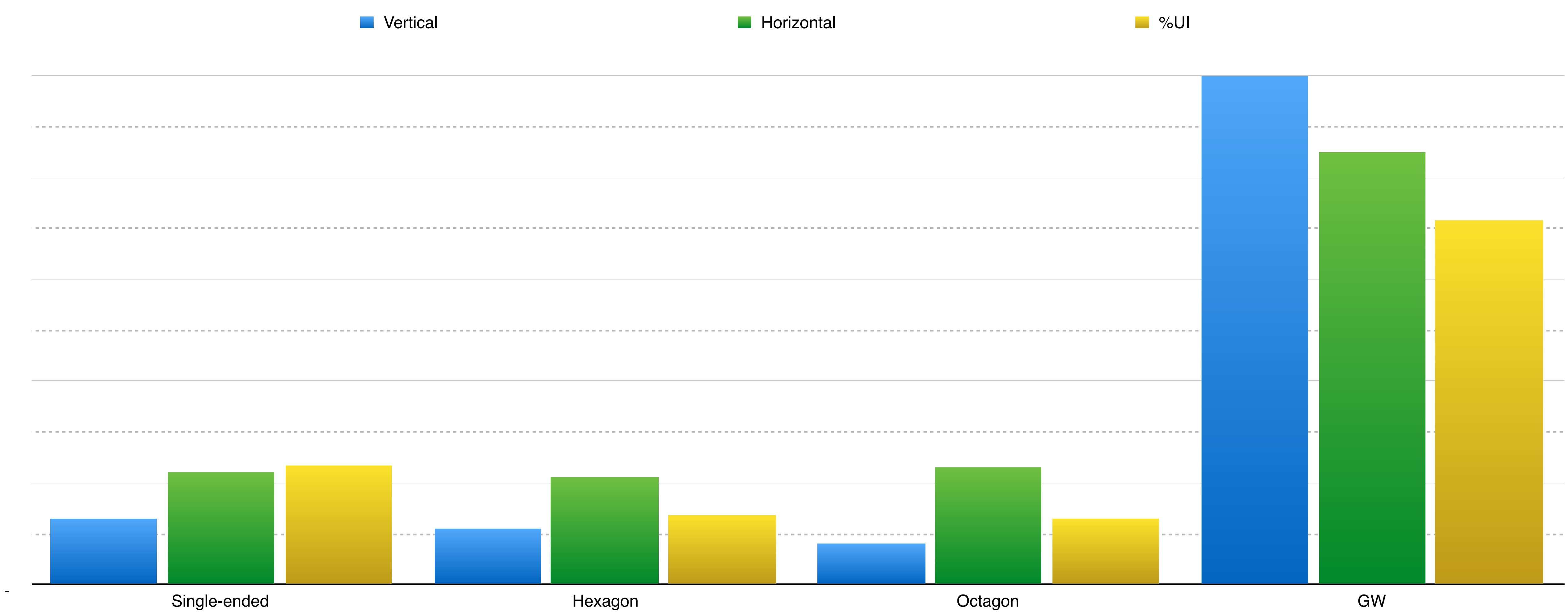
Example: Mobile Memory

Example: Mobile Memory



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Electromagnetic Interference (EMI) Noise

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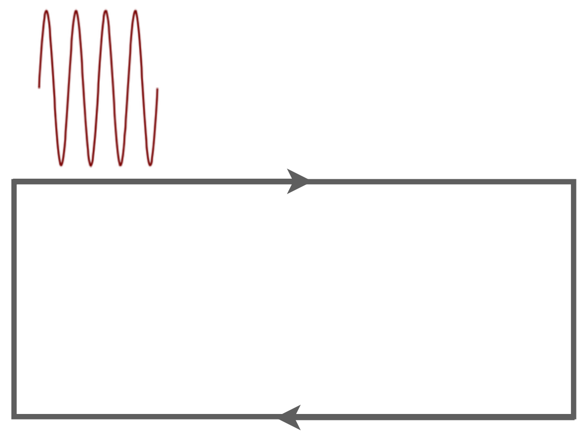
Electromagnetic Interference (EMI)

First order analysis of strength of the Electric far-field generated by a charge loop

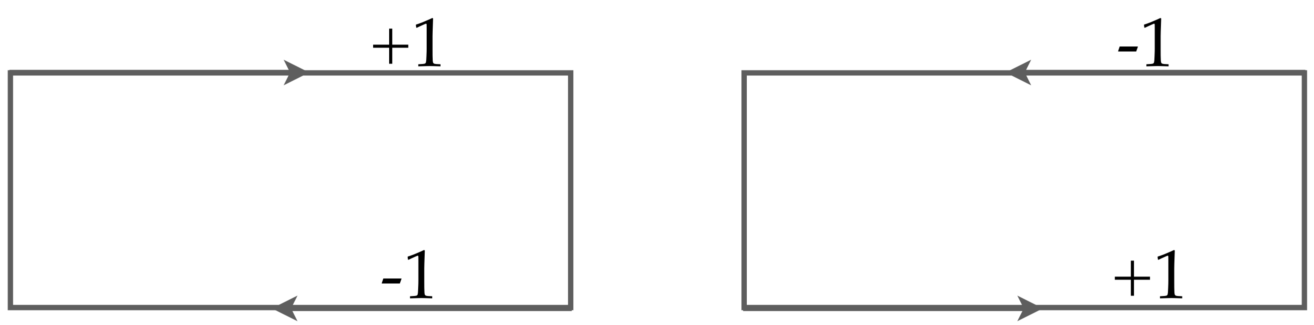


Area = A
Frequency = f
Current = I

Far field strength $\sim f^2 \cdot I \cdot A$

Fix all parameters to 1 for a baseline computation. Then far-field has FOM = 1.

Differential signaling:



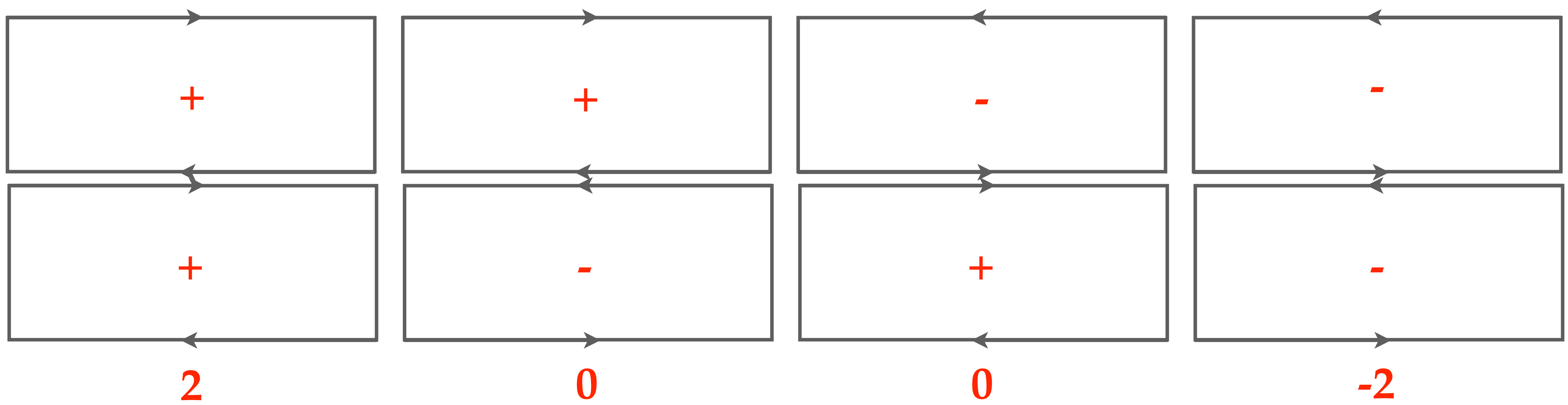
FOM = 1

FOM = -1

Average strength = (1+|-1|)/2 = 1

Electromagnetic Interference

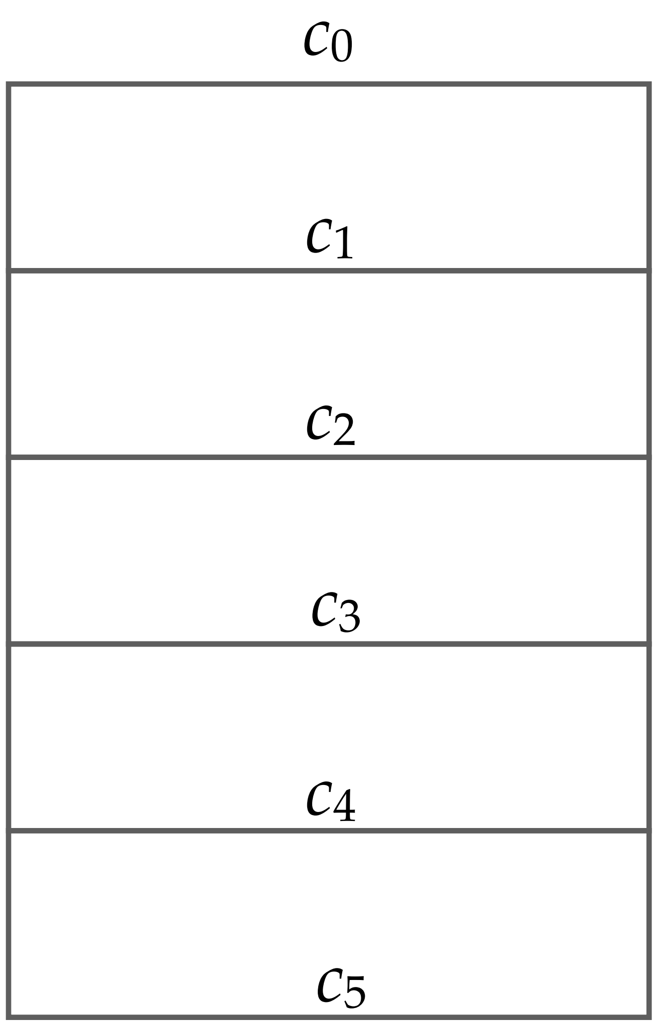
Two differential lanes:



Average strength = (2+|-2|)/4 = 1

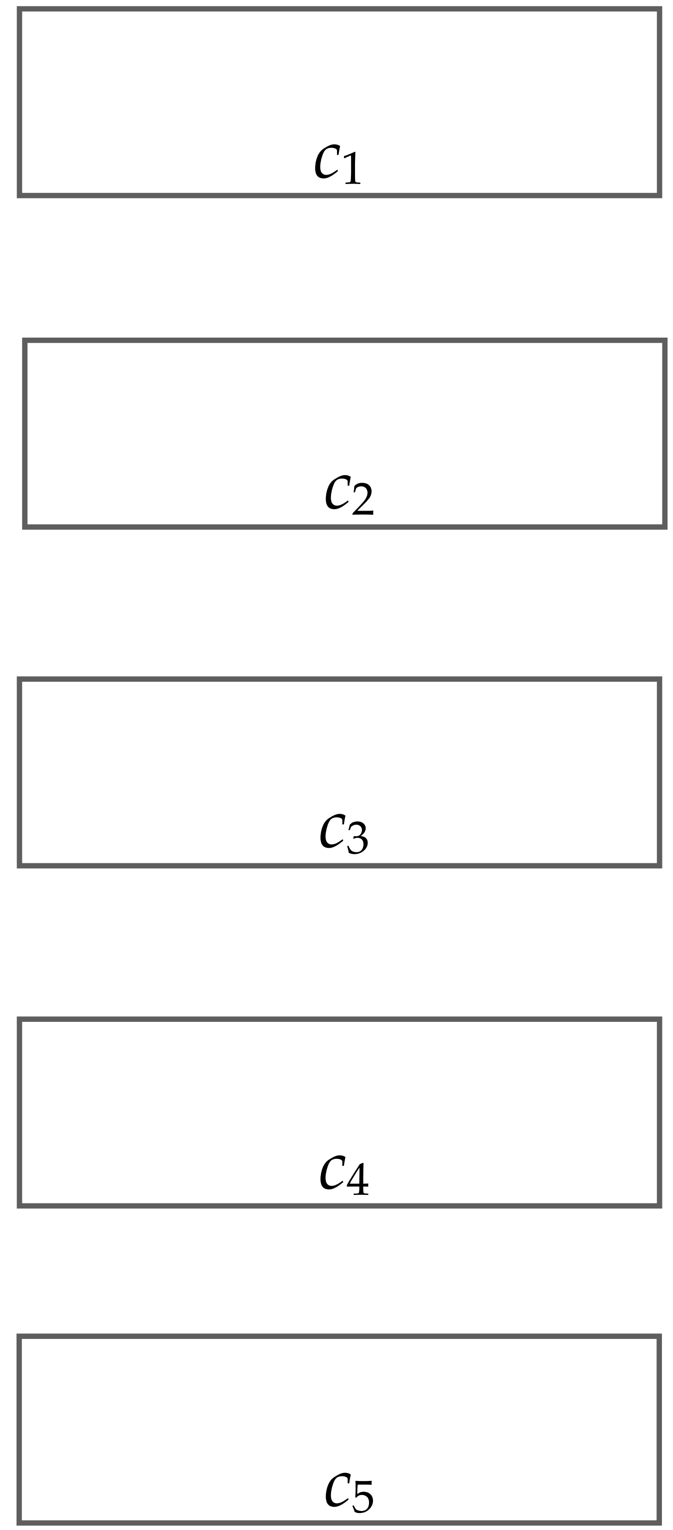
Electromagnetic Interference

General form:



Electromagnetic Interference

General form:



Electromagnetic Interference

General form:

$-c_1-c_2-c_3-c_4-c_5$

$c_1+c_2+c_3+c_4+c_5$

+

$-c_2-c_3-c_4-c_5$

$c_2+c_3+c_4+c_5$

+

$-c_3-c_4-c_5$

$c_3+c_4+c_5$

+

$-c_4-c_5$

c_4+c_5

+

$-c_5$

c_5

Electromagnetic Interference

General form:

$-c_1-c_2-c_3-c_4-c_5$

$c_1+c_2+c_3+c_4+c_5$

$+$

$-c_2-c_3-c_4-c_5$

$c_2+c_3+c_4+c_5$

$+$

$-c_3-c_4-c_5$

$c_3+c_4+c_5$

$+$

$-c_4-c_5$

c_4+c_5

$+$

$-c_5$

c_5

$c_1+c_2+c_3+c_4+c_5$

$+$

$c_2+c_3+c_4+c_5$

$+$

$c_3+c_4+c_5$

$+$

c_4+c_5

$+$

c_5

Electromagnetic Interference

General form:

$-c_1-c_2-c_3-c_4-c_5$

$c_1+c_2+c_3+c_4+c_5$

$+$

$-c_2-c_3-c_4-c_5$

$c_2+c_3+c_4+c_5$

$+$

$-c_3-c_4-c_5$

$c_3+c_4+c_5$

$+$

$-c_4-c_5$

c_4+c_5

$+$

$-c_5$

c_5

$c_1+c_2+c_3+c_4+c_5$

$+$

$c_2+c_3+c_4+c_5$

$+$

$c_3+c_4+c_5$

$+$

c_4+c_5

$+$

c_5

Electromagnetic Interference

$c_1+c_2+c_3+c_4+c_5$

$+$

$c_2+c_3+c_4+c_5$

$+$

$c_3+c_4+c_5$

$+$

c_4+c_5

$+$

c_5

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Electromagnetic Interference

$$c_1+2c_2+3c_3+4c_4+5c_5$$

Electromagnetic Interference

$c'(1)$

Electromagnetic Interference

FOM for a code C in which for all codewords sum of coordinates is zero:

$$\frac{1}{|C|}\sum_{c\in C}|c'(1)|$$

Examples

Two differential lanes: $\frac{1}{4}(2 + |-2|) = 1$

ENRZ: FOM = (2+2/3)/2 = 4/3

$$\pm(1, -1/3, -1/3, -1/3) \to 2$$
$$\pm(-1/3, 1, -1/3, -1/3) \to \frac{2}{3}$$
$$\pm(-1/3, -1/3, 1, -1/3) \to \frac{2}{3}$$
$$\pm(-1/3, -1/3, -1/3, 1) \to 2$$

Equal throughput: differential runs at 1.5 times the frequency. Throughput-normalized FOM:

Differential: $(1.5)^2 = 2.25$ ENRZ: 4/3 ~ 1.33

Examples

Two differential lanes: $\frac{1}{4}(2 + |-2|) = 1$

ENRZ: FOM = (2+2/3)/2 = 4/3

$$\pm(1, -1/3, -1/3, -1/3) \to 2$$

$$\pm(-1/3, 1, -1/3, -1/3) \to \frac{2}{3}$$

$$\pm(-1/3, -1/3, 1, -1/3) \to \frac{2}{3}$$

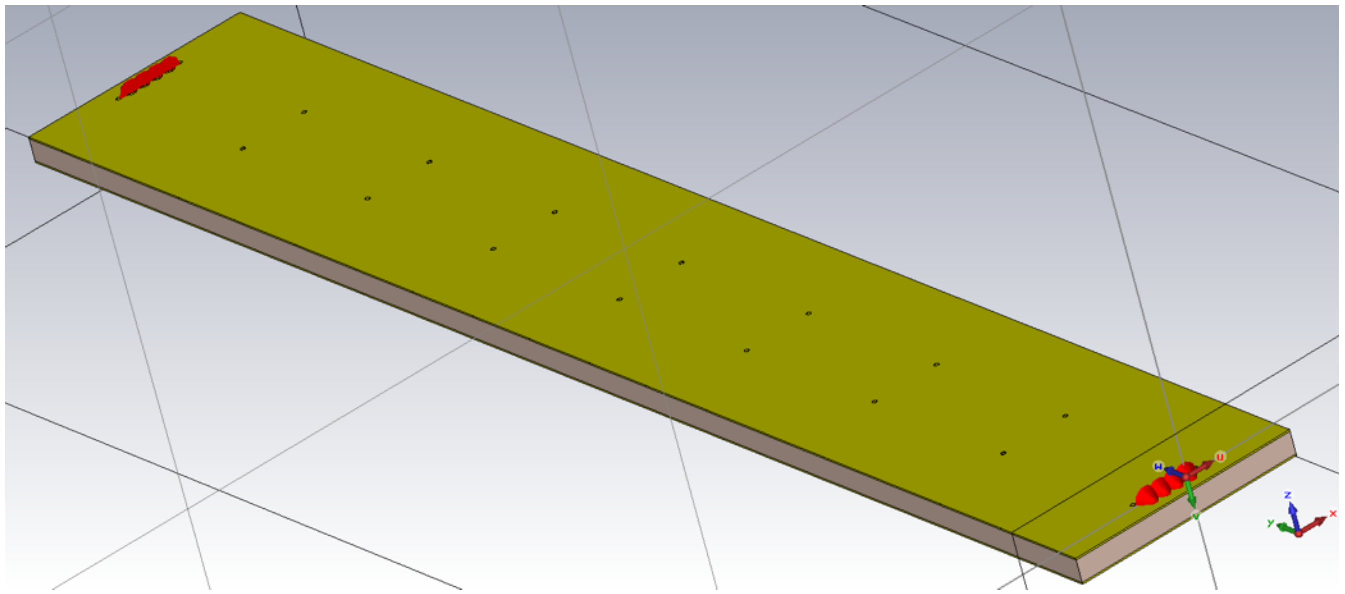
$$\pm(-1/3, -1/3, -1/3, 1) \to 2$$

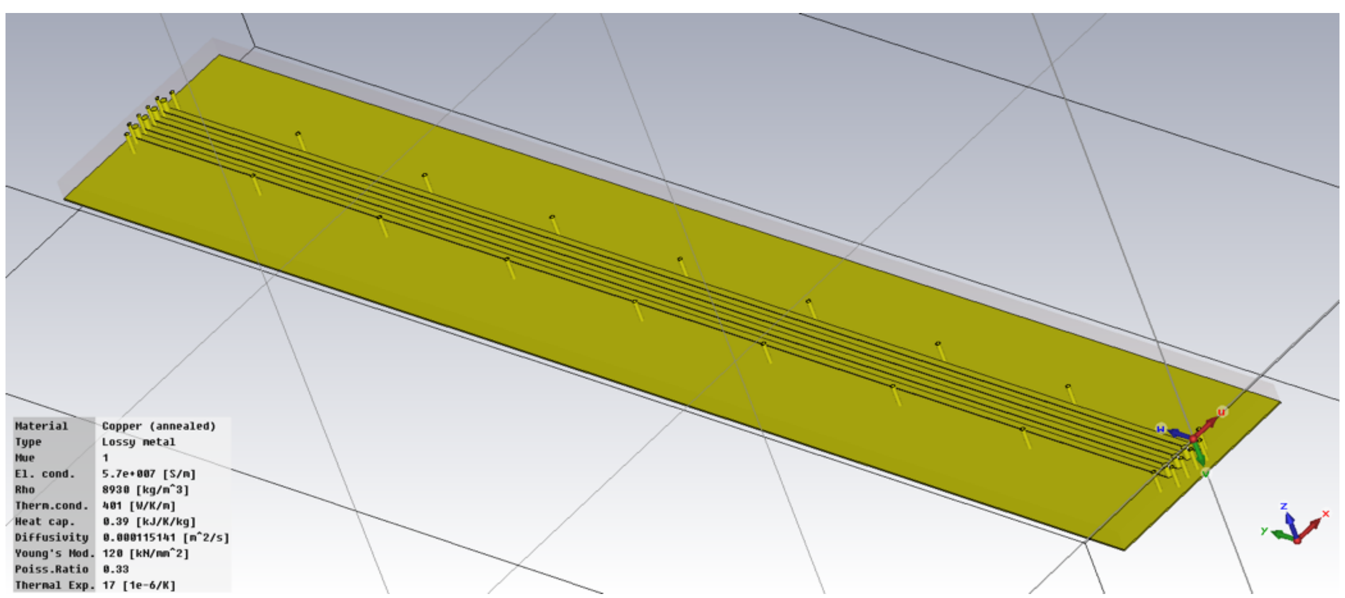
Equal throughput: differential runs at 1.5 times the frequency. Throughput-normalized FOM:

Differential: $(1.5)^2 = 2.25$ ENRZ: 4/3 ~ 1.33

SMALLER!

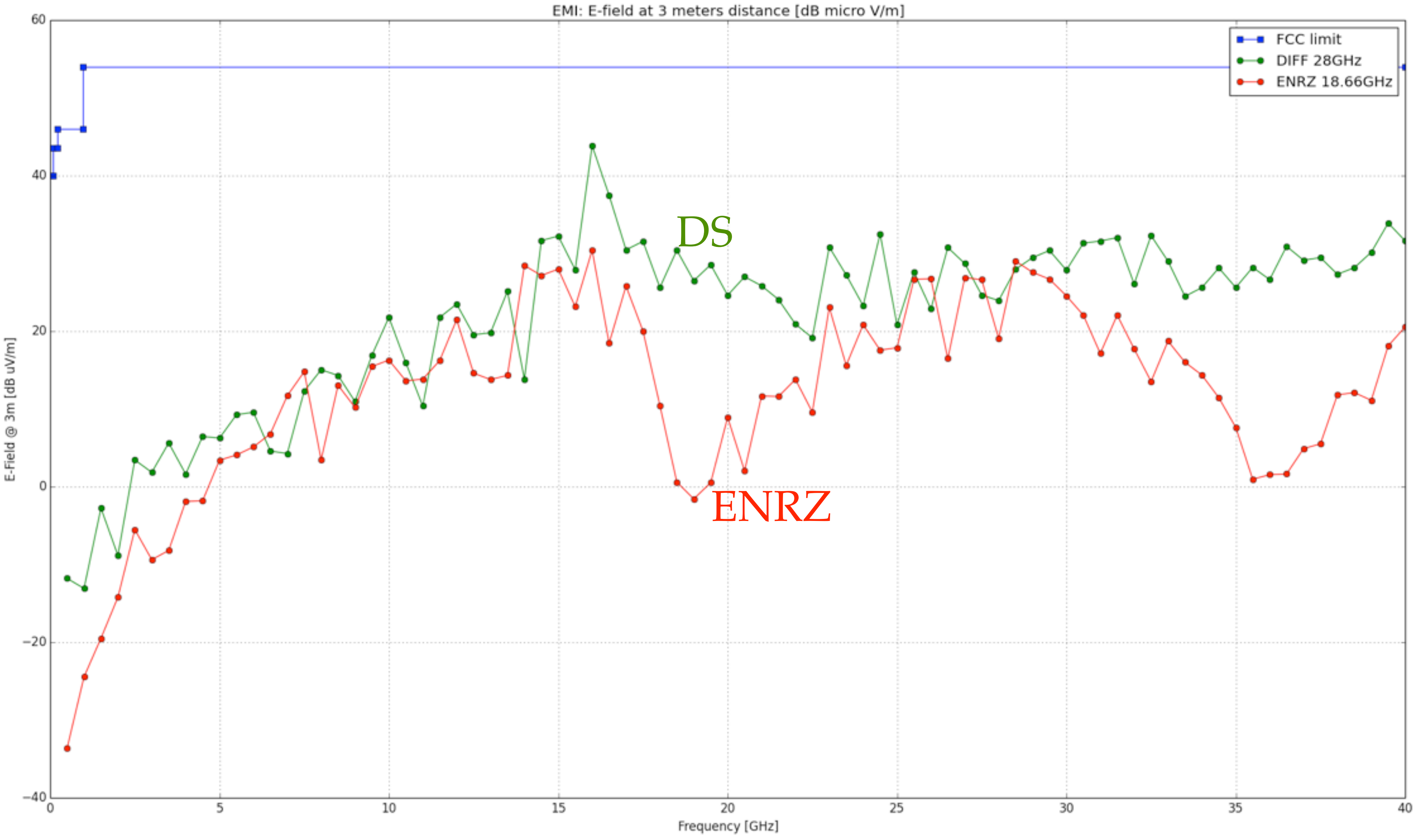
E-Field of ENRZ





- Equidistant traces
- 150 µm of spacing
- 150 µm wide
- Copper material
- Wires (30cm) are shielded, emissions caused by the wire traces connecting to vias
- 112 Gbps over four wires
  - 28 GHz clock for differential signaling
  - 18.66 GHz clock for ENRZ

E-Field of ENRZ



Full Design

Design Problems

- Given n and N, design a chordal code such that
  - The ISI-ratio is as small as possible (ISI noise)
  - The spread of the L1-norm of the codewords is small (SSO noise)
  - The coordinates of the codewords and of the comparators sum up to zero (CM noise)
  - The absolute value of the derivatives of the codewords at 1 is small (EMI noise)
  - The L1-norm of the codewords is small (power consumption on the wires)
  - The L2-norm of the codewords is small (small termination power)
  - The number of comparators is as small as possible
  - The alphabet size is as small as possible
  - There are as few as possible inactive pairs
  - The encoder is "simple"
  - The decoder is "simple"

- Some of these problems can be reduced to combinatorial optimization problems.

Chordal Codes: Omitted Topics

- Chordal coding
  - Theory of multi-referenced chordal codes
  - Theory of transition limiting chordal codes (CMOS driver)
  - Theory of clock embedded chordal codes
  - Combinatorial code design techniques
  - Asymmetric coding
  - Comparator minimization techniques
  - Mismatch tolerance techniques
  - SSO reducing centrally referenced chordal codes
  - Combinatorial quantization techniques
  - Chordal codes with different detectors
  - Multi-tone chordal codes
  - Algorithm design techniques
  - and more....
- Signal integrity
  - Matched low power CTLE, FIR, DFE
  - Coded low power CDR
  - Efficient board routing
  - Skew compensation circuits
  - SSO reduction circuits matched to chordal coding
- Matching circuits, Tx and Rx topologies,...

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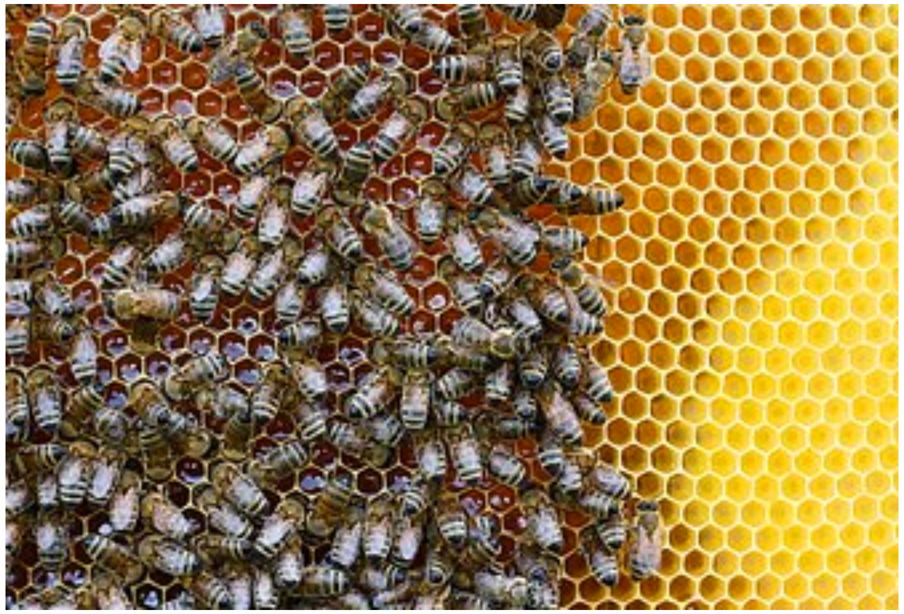

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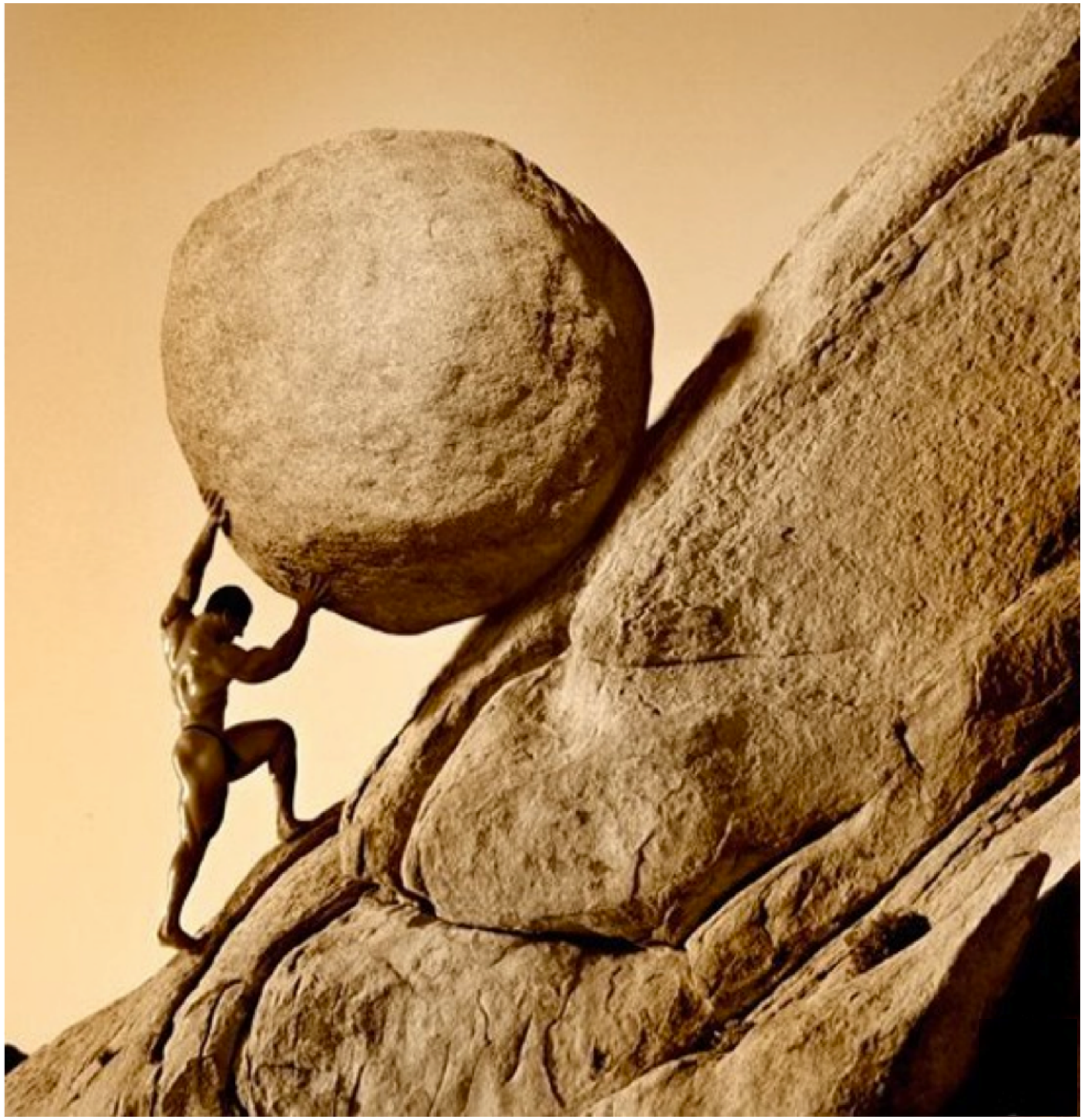
But…

But…

La lutte elle-même vers les sommets suffit à remplir un cœur d'homme.
Il faut imaginer Sisyphe heureux.
-- Albert Camus, “Le Mythe de Sisyphe”



The struggle itself toward the heights is enough to fill a man’s heart.
One must imagine Sisyphus happy.
-- Albert Camus, “The Myth of Sisyphus”

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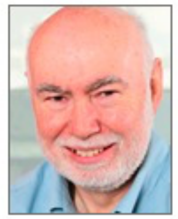



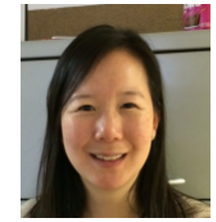



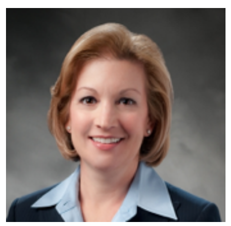


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reinventing the

BUS