Chordal Codes

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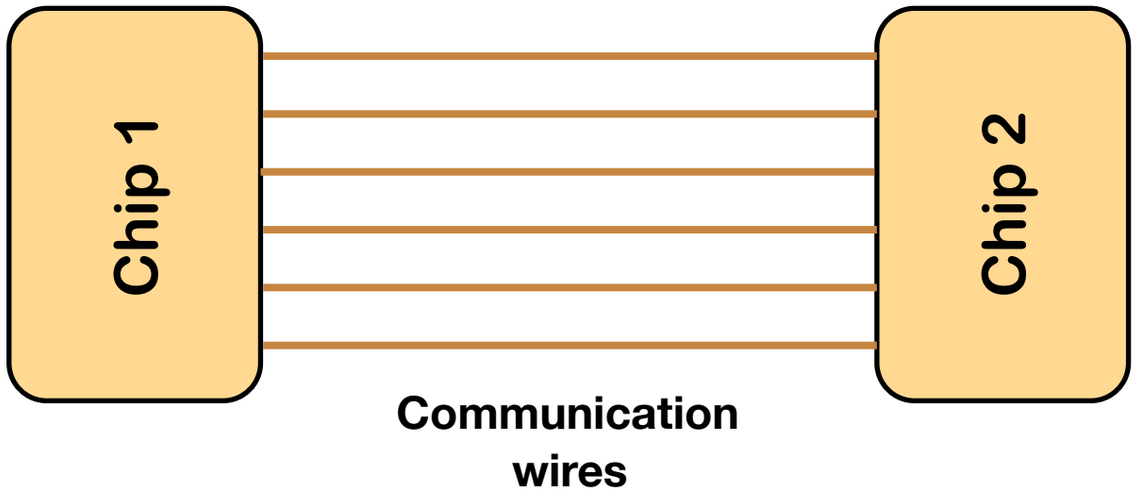
KANDOU BUS

ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

Chip-to-Chip Communication

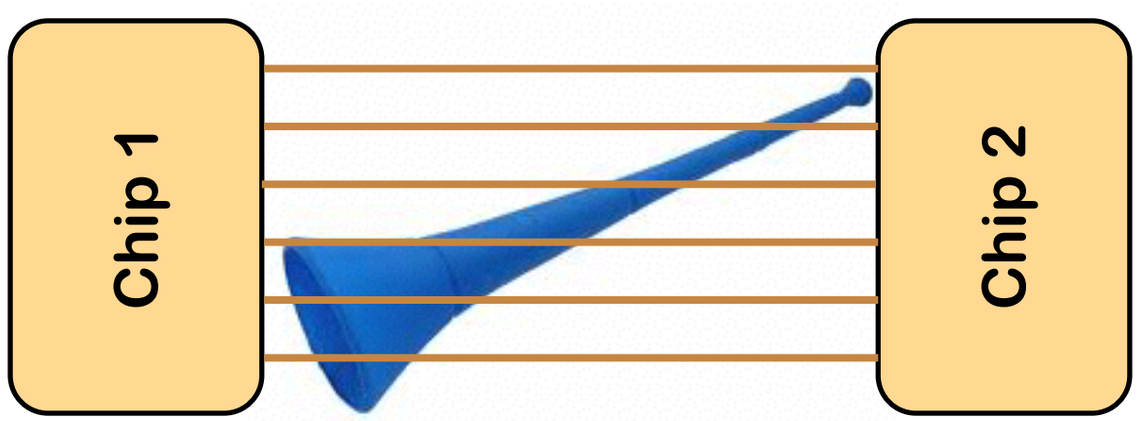


Task: reliably transmit information from Chip 1 to Chip 2

Chip-to-Chip Communication

- We see them everywhere.

Noise



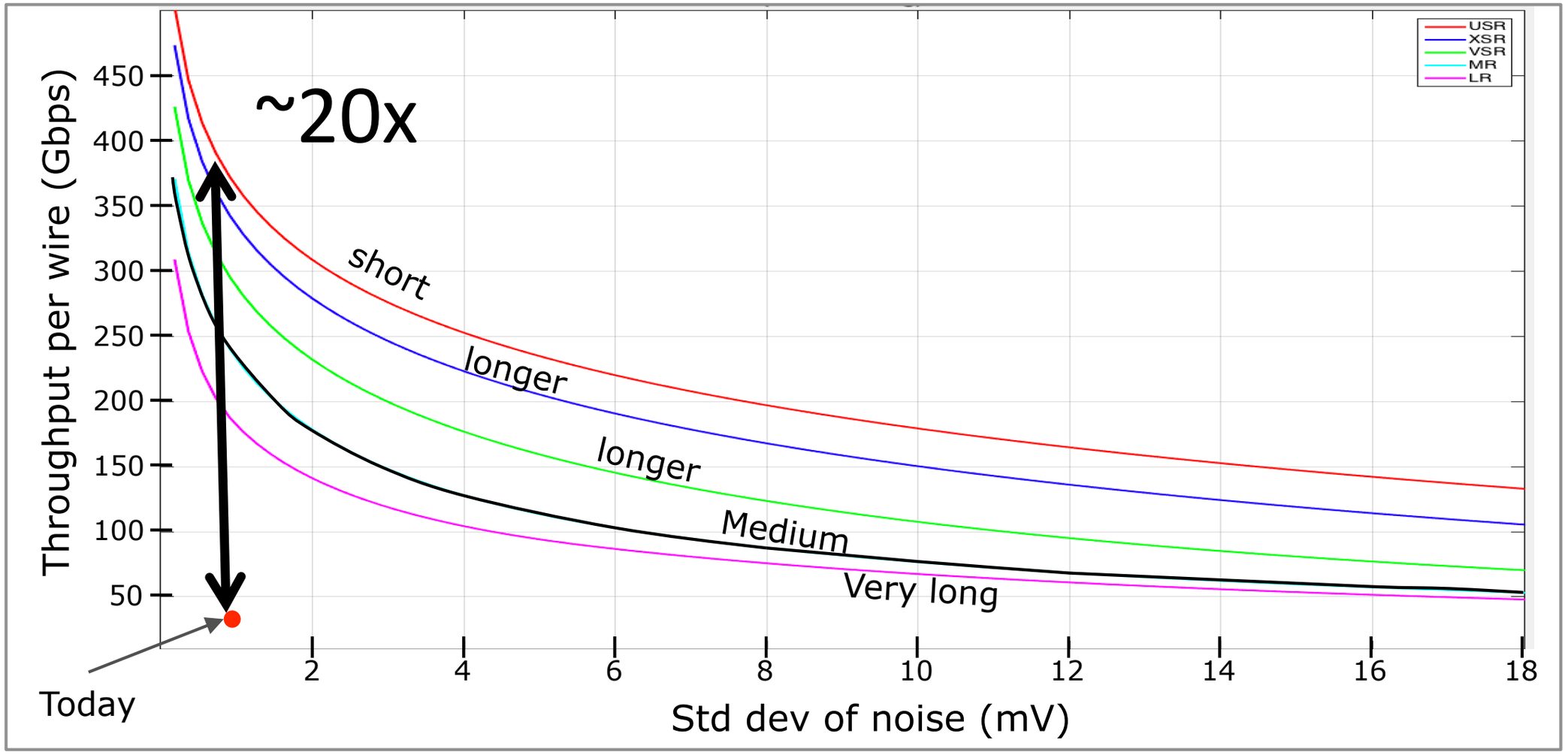
Noise scales badly with frequency of transmission:
Example: -40dB at frequency *f*, -90dB at *2f*

Power

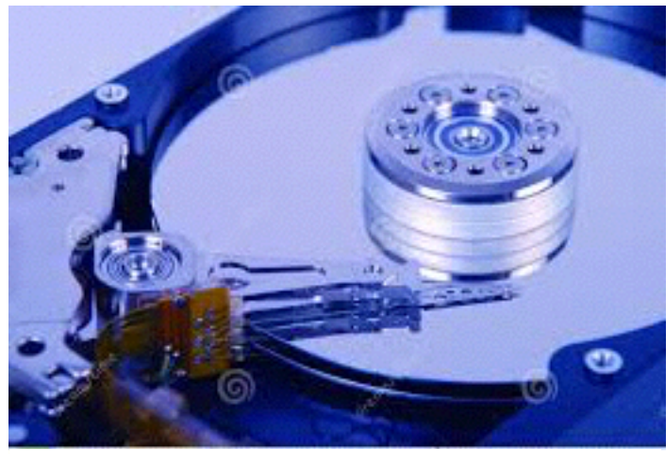
	Supercomputers	Data centers
Internal traffic in Giga-bits per second	1E+12	4E+11
Power in Mega-Watts	20000	8000

Multiply by 4 in every generation (~2 years)
Very partially offset by Moore's law

Information Theory

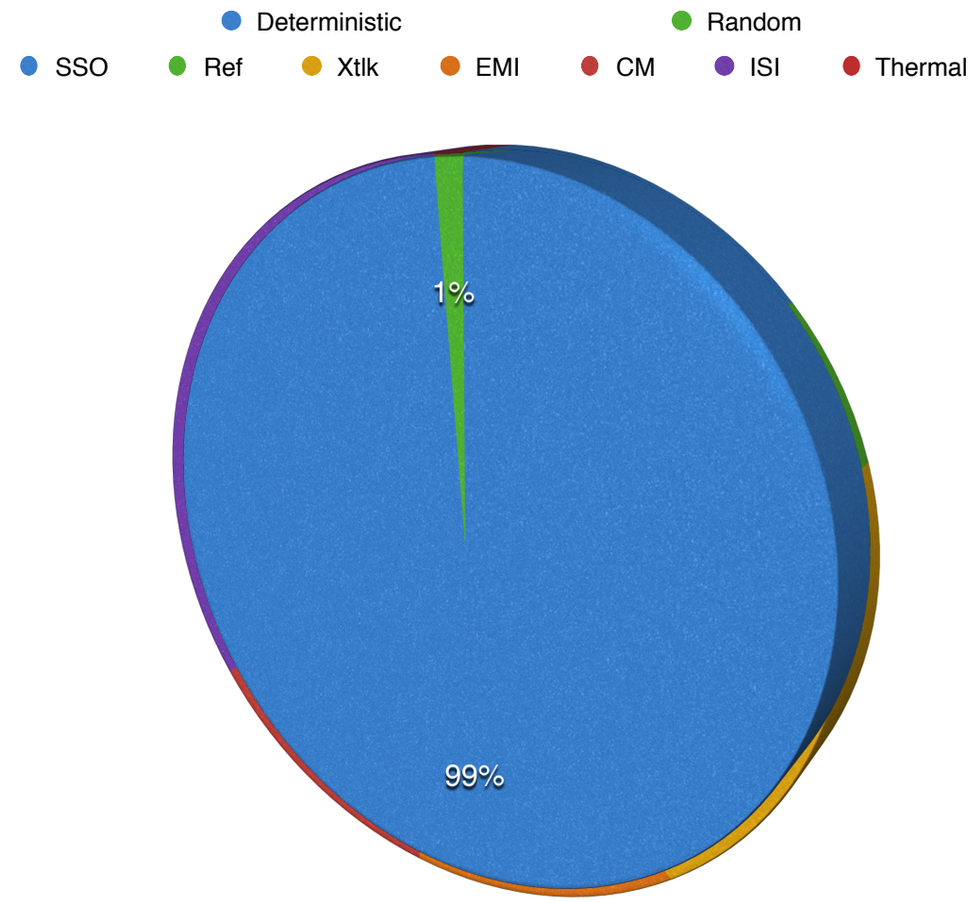


What Chip-to-Chip Channels are NOT



Or any channel with a lot of “random” noise

Noise



Almost all the noise is deterministic
but resources are tight

Rule of Thousands

	Throughput	Energy/bit	Recovery time/ bit
Wireless	Mbps	nJ	nano-second
Chip-to-Chip	Gbps	pJ	pico-second

Hardly any power or time to recover a transmitted bit

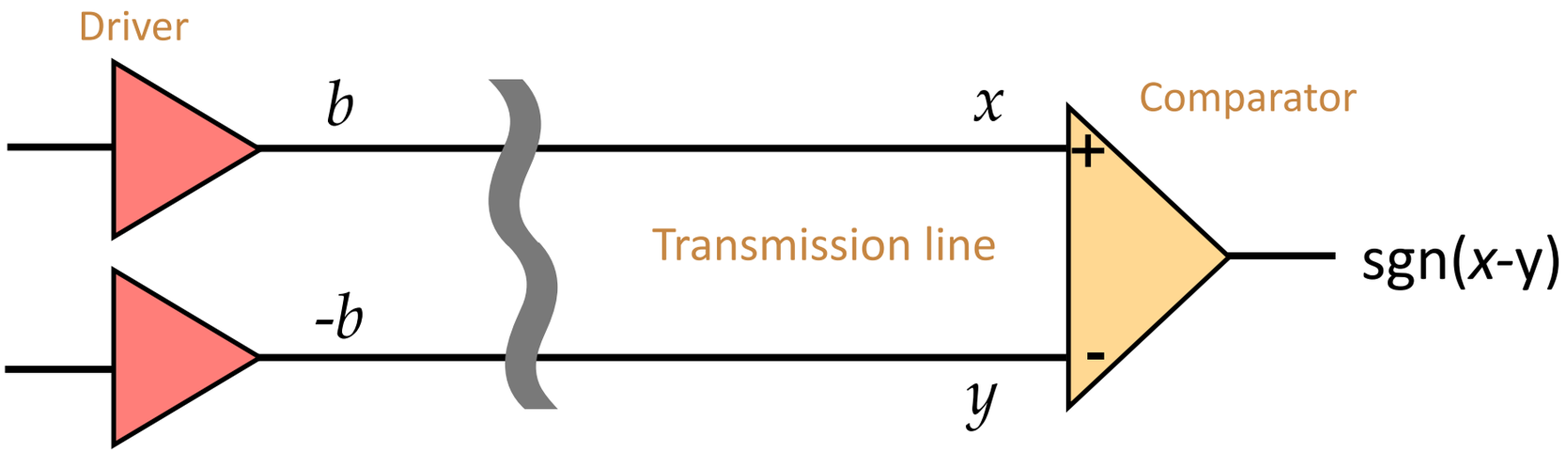
Theory of Chord Signaling

Noise Types

- Simultaneous Switching Output (SSO) noise
- Reference noise
- Crosstalk
- Electromagnetic Interference (EMI) noise
- Common Mode (CM) noise
- Inter-symbol Interference (ISI) noise
- Thermal noise

Create a coding/modulation scheme that is resilient to all of these noise types

Differential Signaling

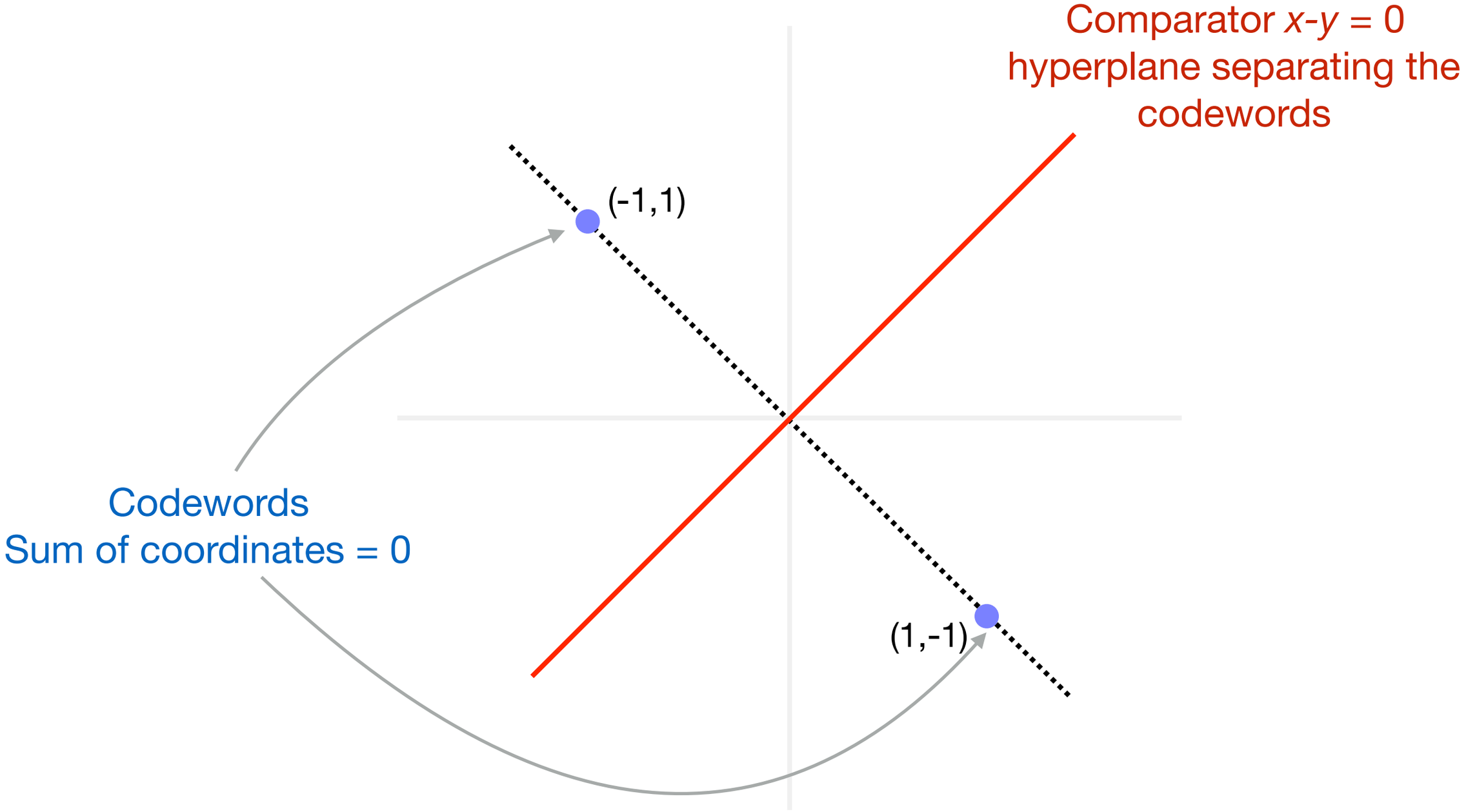


Transmits one bit per *a pair* of wires

Differential Signaling

Bread and butter of virtually ALL high-speed links anywhere

Geometric Perspective



Code = Codewords + Comparator

(Some) Properties

Property	Note
Sum of coordinates of codewords = 0	Common mode resilience
Comparator vanishes at (1,1)	Common mode resilience
Codewords are on opposite sides of comparator	Comparator distinguishes codewords
Wire values are binary	Easier implementation
L1-norm of codewords is constant	Resilience to SSO noise
Transmits one bit on two wires	Needs higher clock rate

Chordal Code - First Attempt

A (*n, N, c*)-*Chordal Code* (CC) is a pair (C, Λ) where

- *C* is a subset of $[-1, 1]^n$ of size *N* (set of codewords on *n* wires)
- Λ is a subset of $(\mathbb{R}^n)^*$ of size *c* (set of comparators)

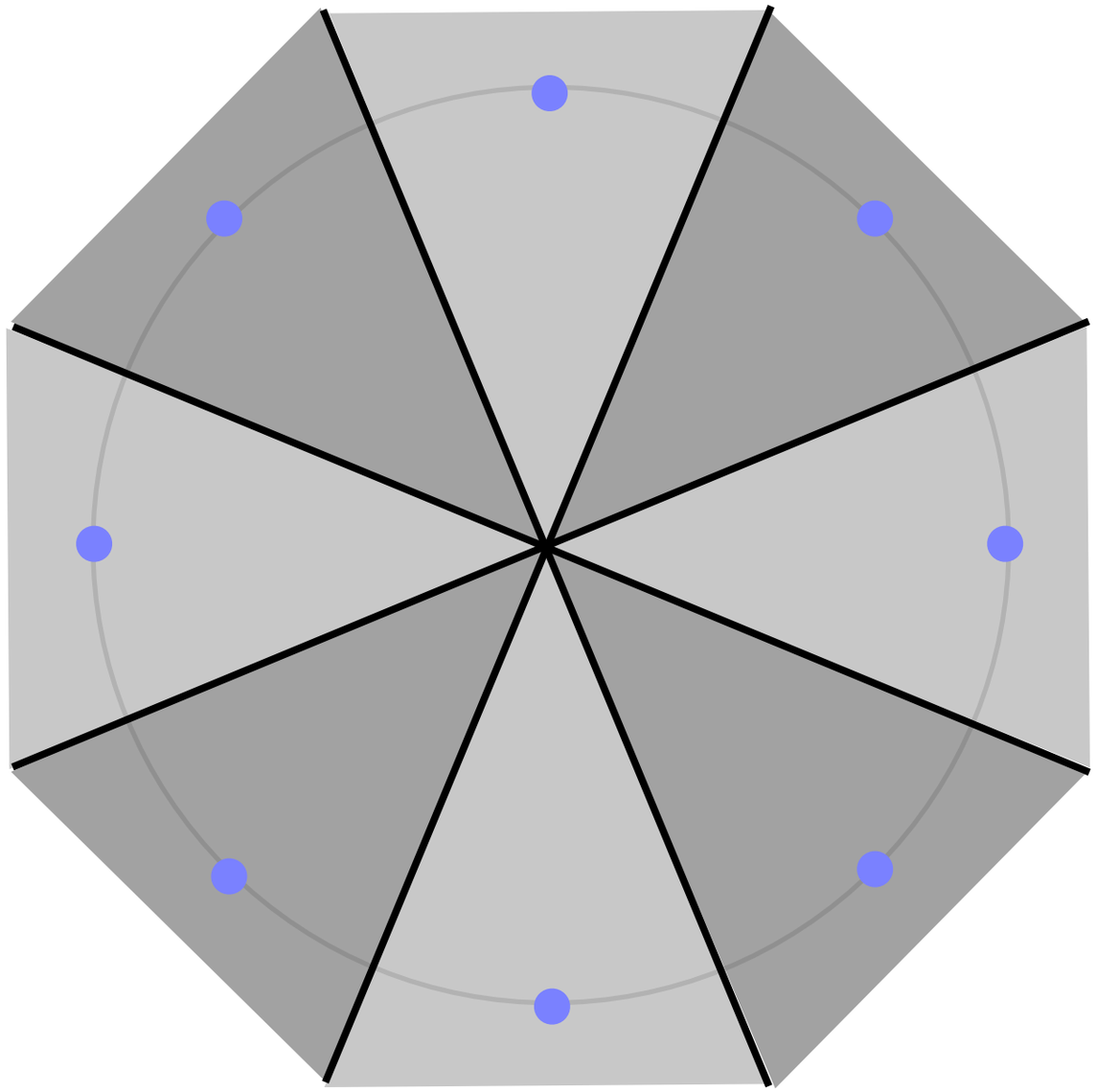
such that

- The coordinates of all codewords sum to zero
- The comparators vanish on (1,1,…,1).
- The L1-norm of the codewords is fixed (or has small variation)
- (Distinguishibility) $\forall c_1, c_2 \in C, c_1 \neq c_2 \exists \lambda \in \Lambda : \lambda(c_1)\lambda(c_2) < 0$

$\frac{\log_2(N)}{n}$ is called the *rate* of the code (or *pin-efficiency*)

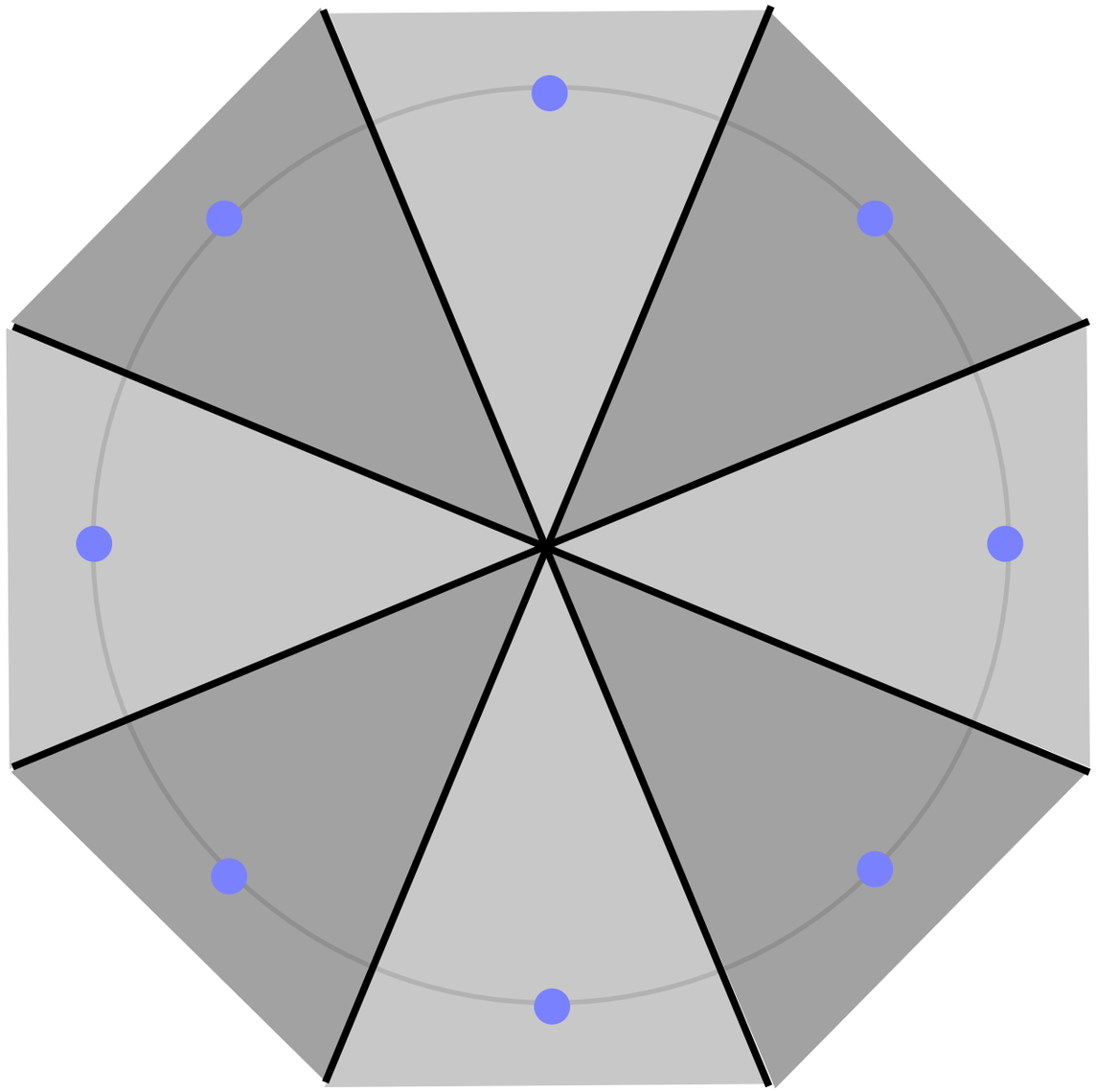
Given *n* and *N,* find minimum *c*, such that there exists a (*n, N, c*)-CC.

3 Bits, 2 Wires

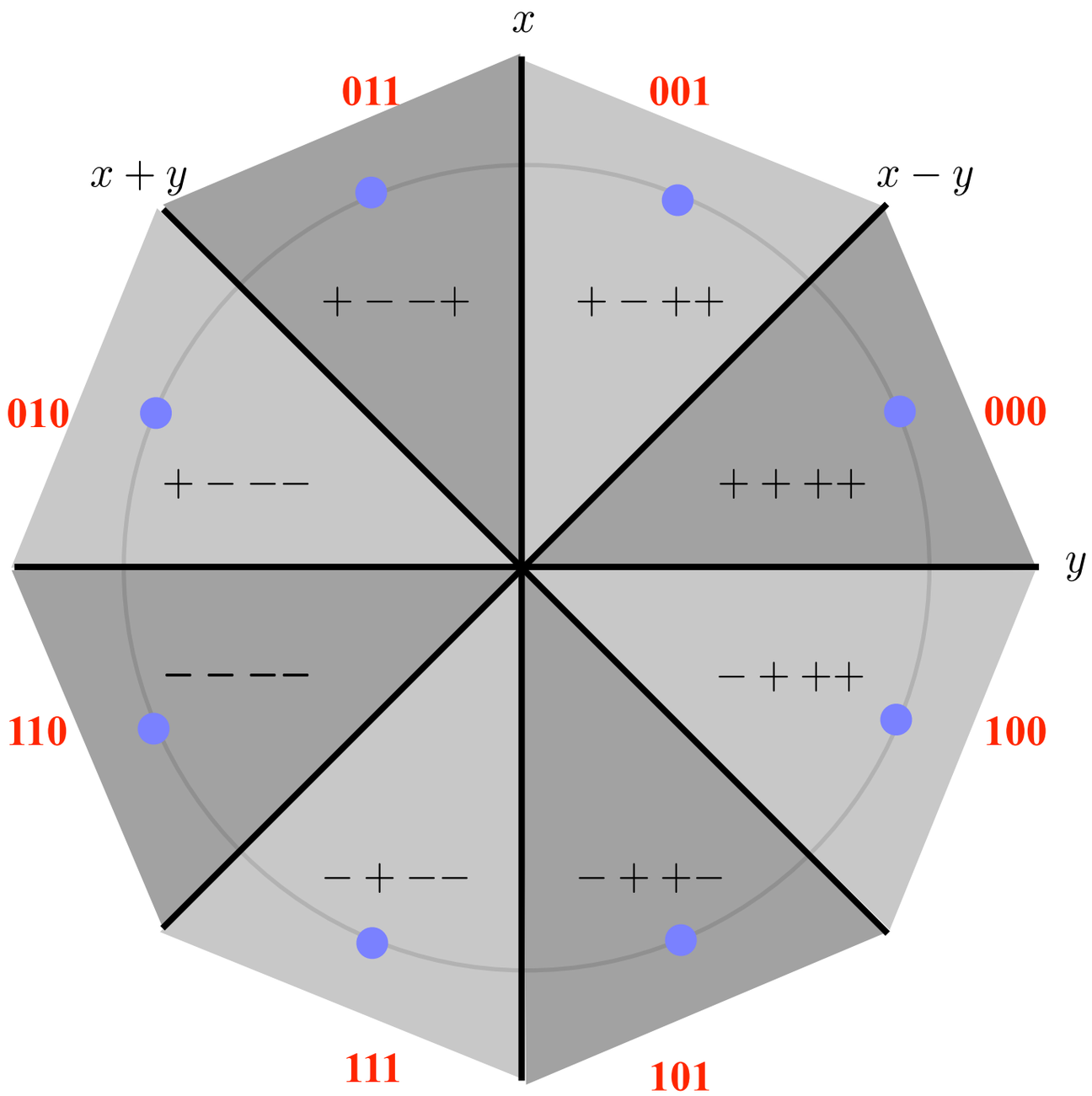


Sum is not zero, but don’t worry about that!

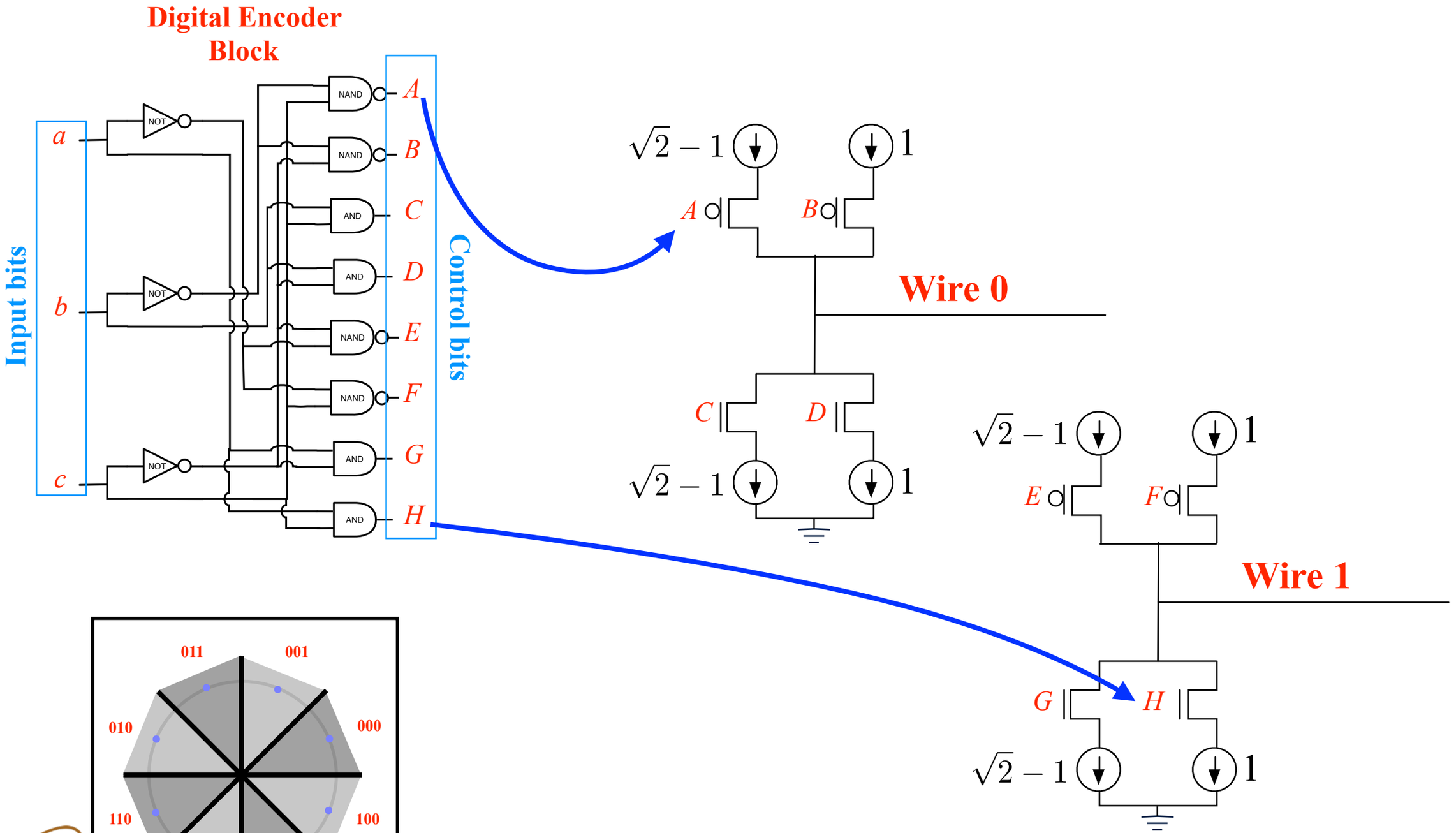
3 Bits, 2 Wires

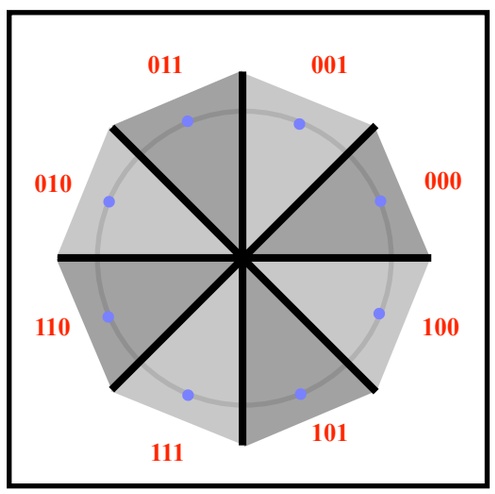


3 Bits, 2 Wires

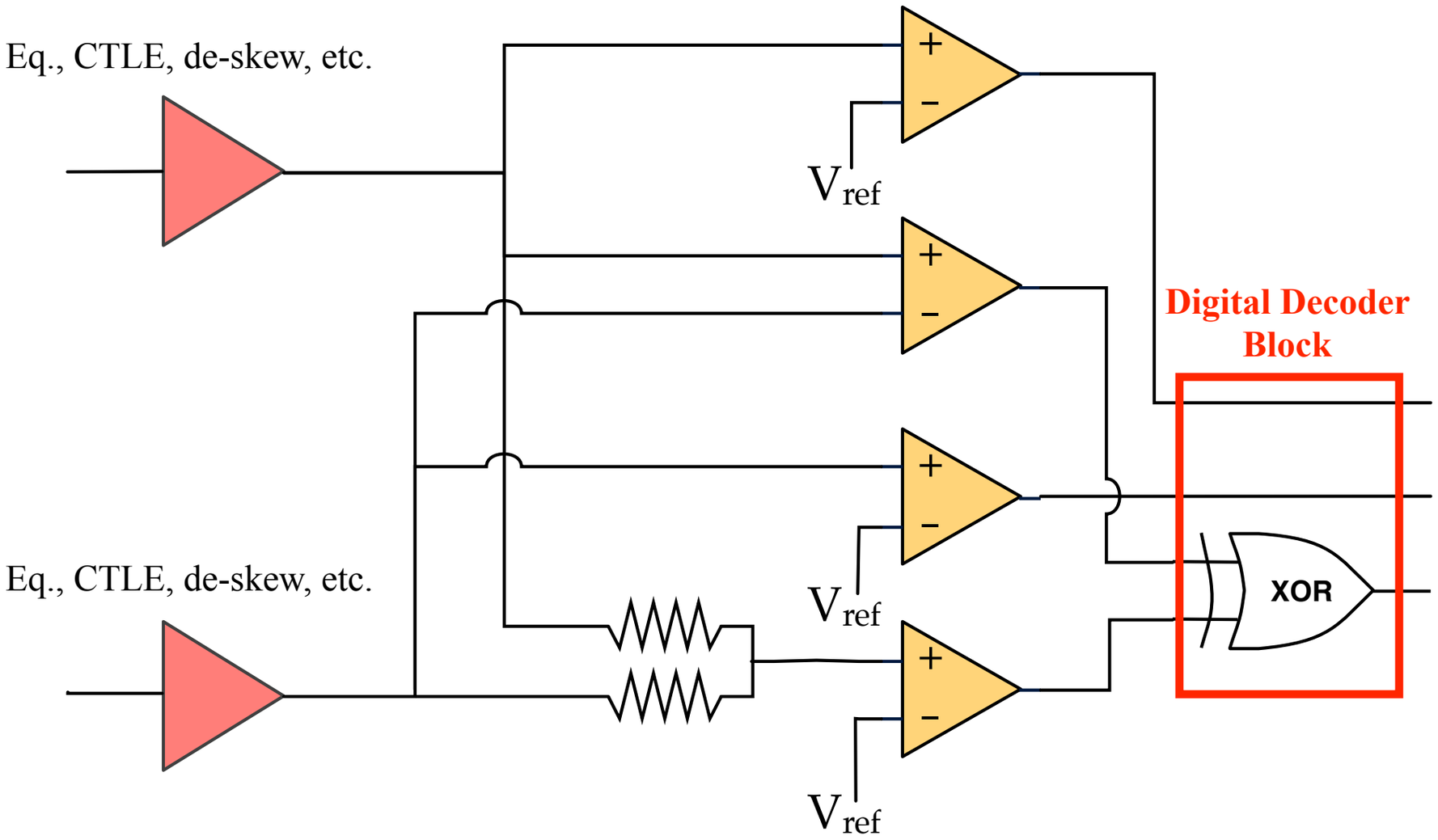


Driver, Encoder





Receiver, Decoder



Decoding Algorithm

Chordal codes are born with an efficient “decoding algorithm” (Comparators are part of the definition)

The situation is similar to LDPC codes where efficient algorithms are at the foreground.

LDPC codes are chosen so that the algorithm performs well.

Very similar in the context of chordal codes.

Zaslavsky's Theorem (+something)

$$N \leq \sum_{i=0}^{n} \binom{c}{i} (1 + (-1)^{n-i})$$

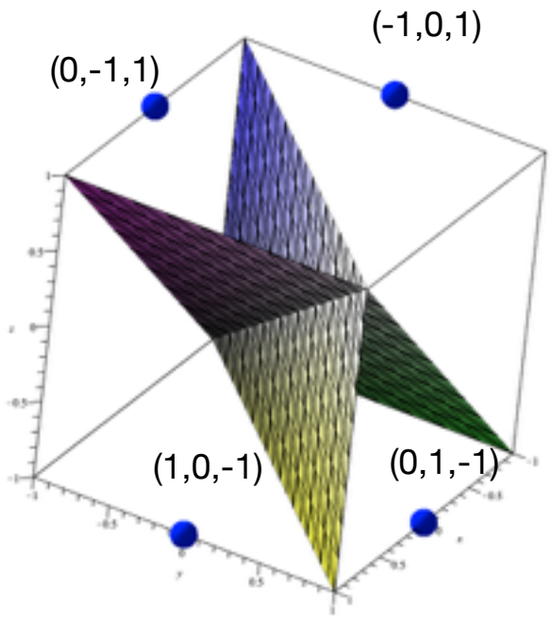
rate can be arbitrarily large at the expense of number of comparators

Example:

n = 3 (3 wires), c = 2 (2 comparators)

$N \leq 4$ so at most 4 codewords

Examples

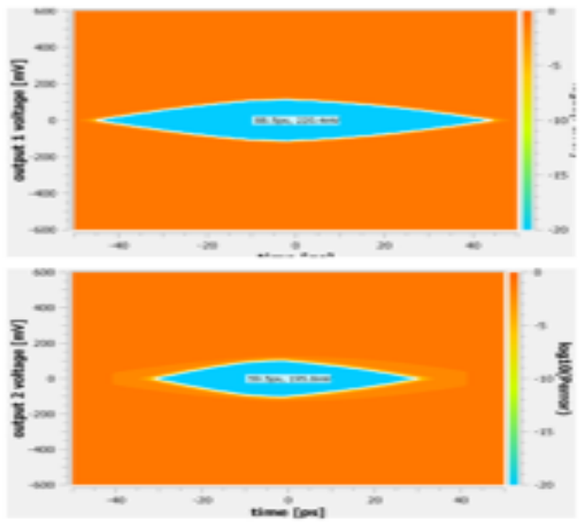


Comparators

Codewords

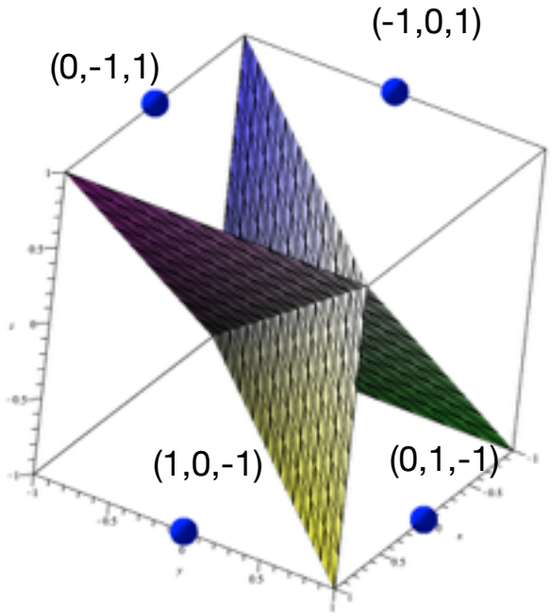
	1,-1,0	1,0,-1
0,-1,1	+1	-1
-1,0,1	-1	-2
1,0,-1	+1	+2
0,1,-1	-1	+1

1,-1,0



1,0,-1

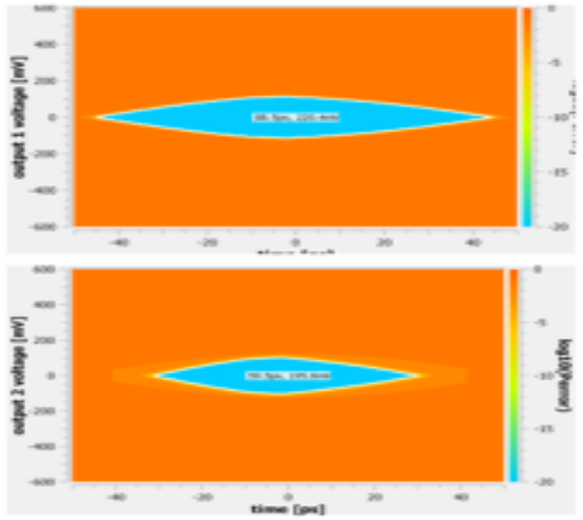
Examples



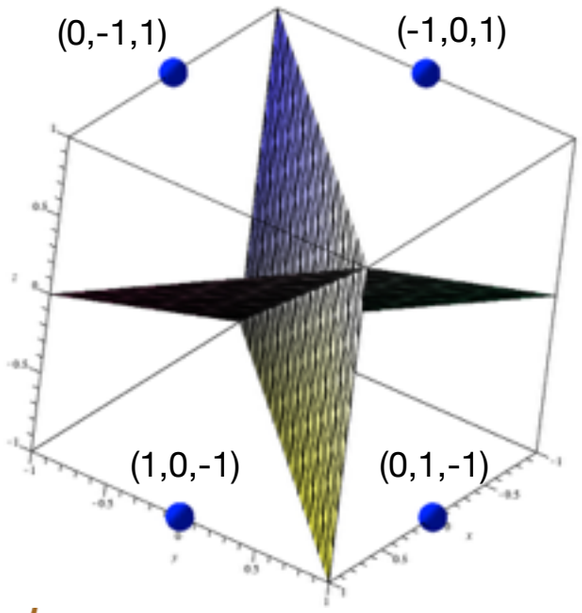
Comparators

Codewords	1,-1,0	1,0,-1
0,-1,1	+1	-1
-1,0,1	-1	-2
1,0,-1	+1	+2
0,1,-1	-1	+1

1,-1,0



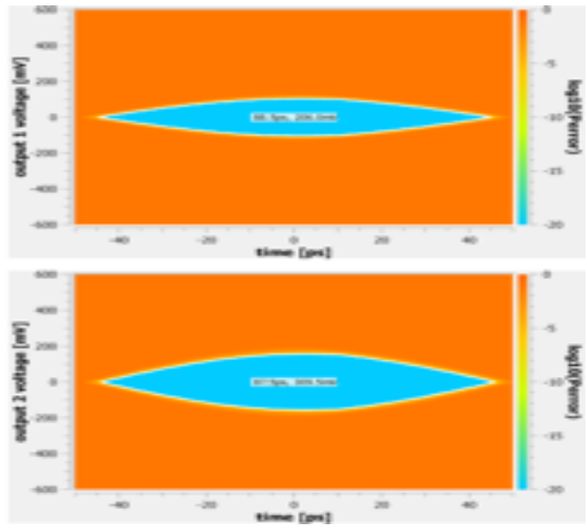
1,0,-1



Comparators

Codewords	1,-1,0	1/2,1/2,-1
0,-1,1	+1	-3/2
-1,0,1	-1	-3/2
1,0,-1	+1	+3/2
0,1,-1	-1	+3/2

1,-1,0



1/2,1/2,-1

Noise Types

- Simultaneous Switching Output (SSO) noise
- Reference noise
- Crosstalk
- Electromagnetic Interference (EMI) noise
- Common Mode (CM) noise
- Inter-symbol Interference (ISI) noise
- Thermal noise

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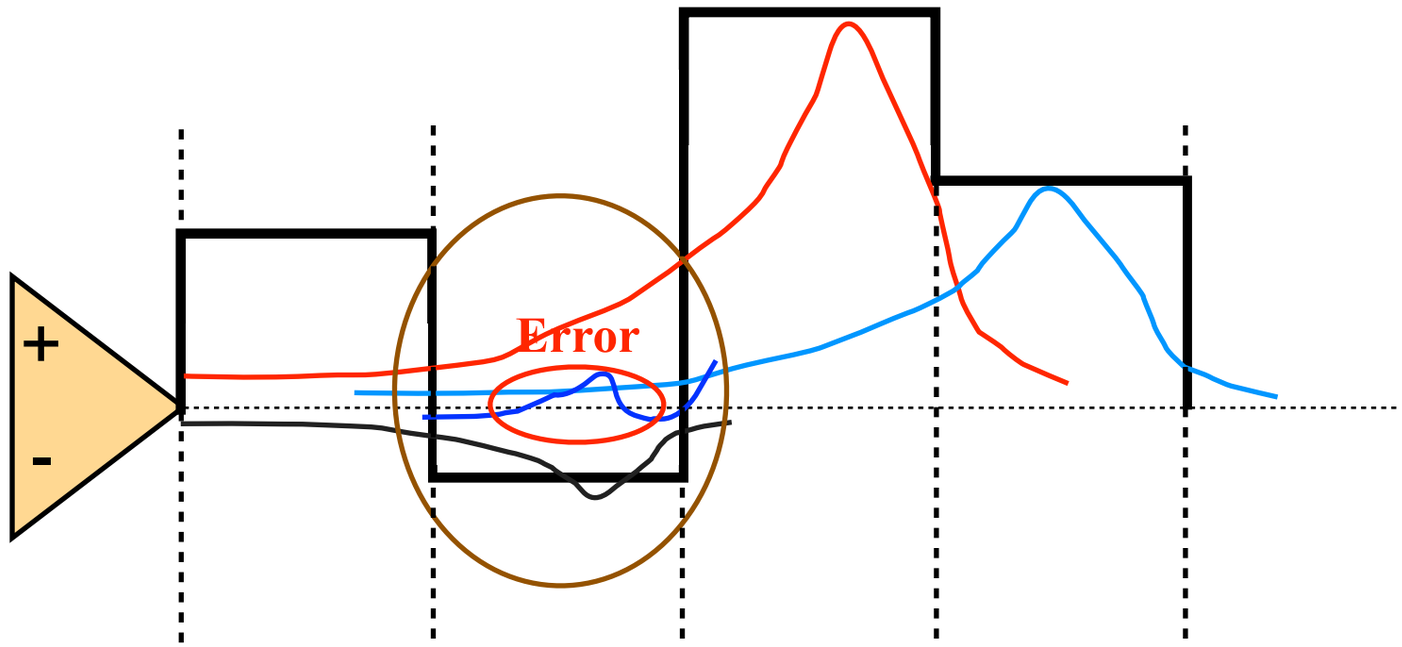
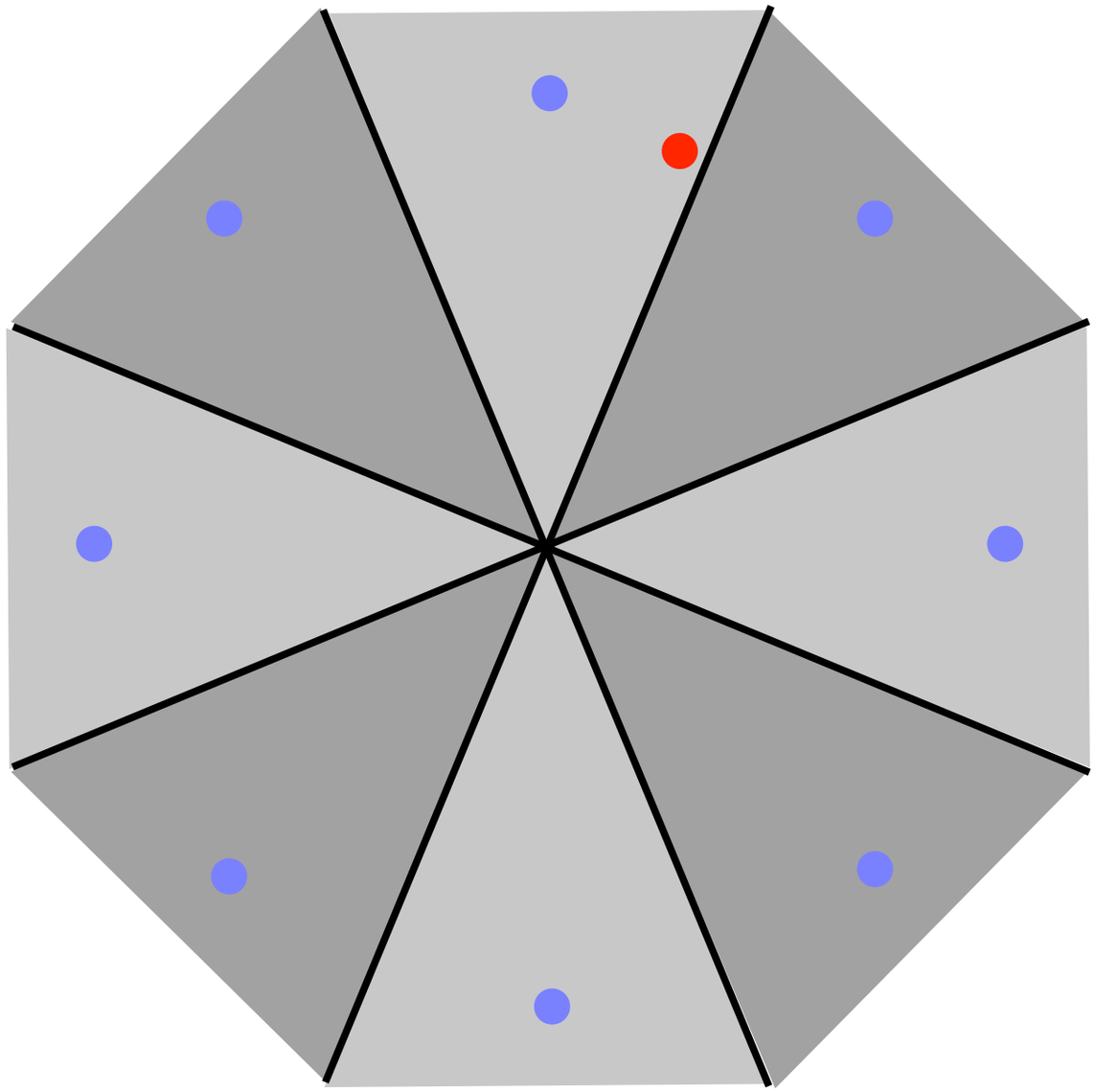
Intersymbol-Interference



Leads to horizontal closure of the eye

Geometric Interpretation



ISI-Ratio

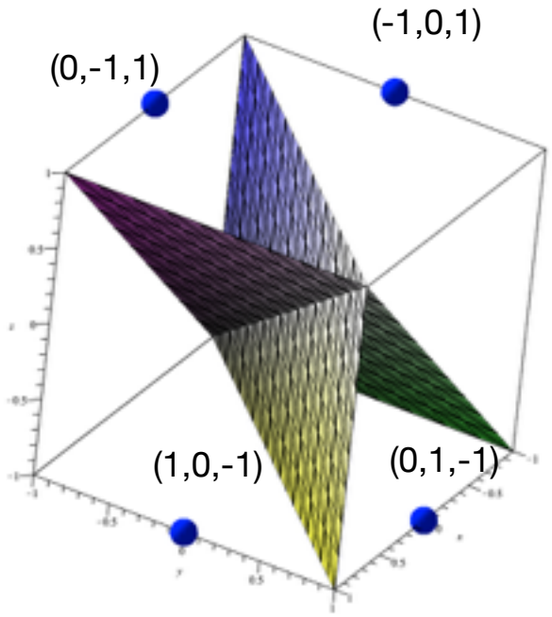
λ comparator for code *C,* assume that λ(*c*) nonzero for all *c* in *C*.

- *ISI-ratio* of λ w.r.t. *C* is $\frac{\max_{c \in C} |\lambda(c)|}{\min_{c \in C} |\lambda(c)|}$
- The *ISI-ratio* of an (*n,N,c*)-CC is the <u>maximum</u> of the ISI-ratios of its comparators.

The larger the ISI-ratio is, the more susceptible is the chordal code to ISI.

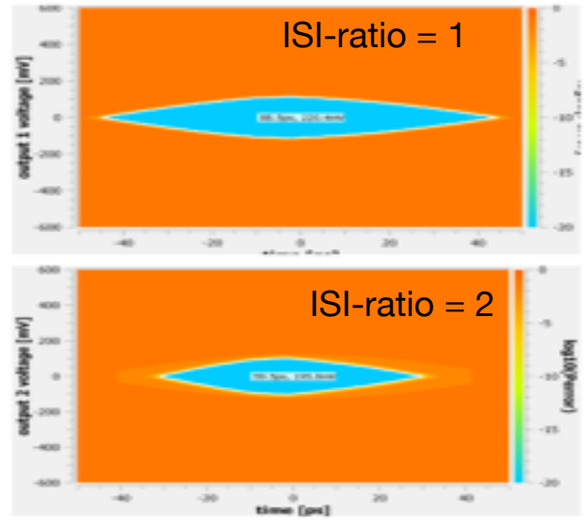
The larger the ISI-ratio, the smaller the horizontal opening of the eye (and the less the tolerance of the system to clock jitter)

Examples



Comparators

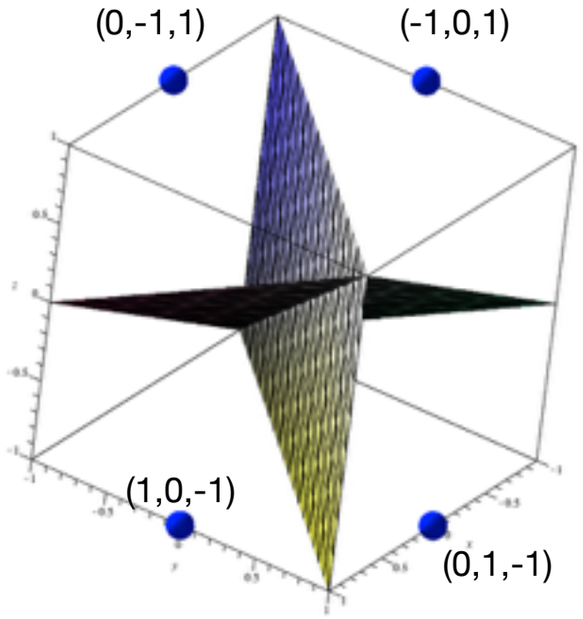
Codewords	1,-1,0	1,0,-1
0,-1,1	+1	-1
-1,0,1	-1	-1
1,0,-1	+1	+1
0,1,-1	-1	+1



ISI-ratio = 1/1 = 1
Horiz. opening larger

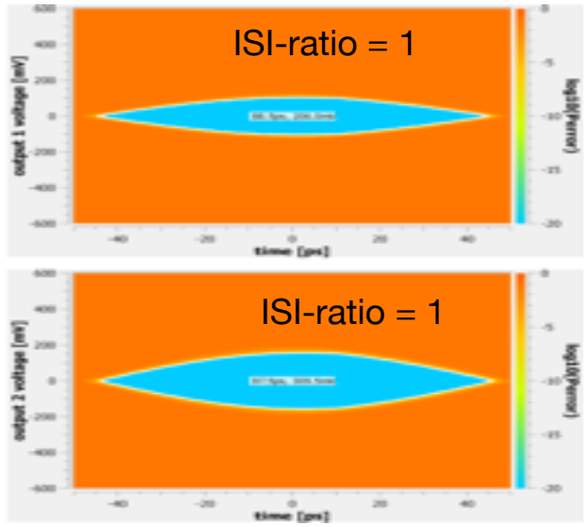
ISI-ratio = 2/1 = 2
Horiz. opening smaller

Examples



Comparators

Codewords	1,-1,0	1/2,1/2,-1
0,-1,1	+1	-3/2
-1,0,1	-1	-3/2
1,0,-1	+1	+3/2
0,1,-1	-1	+3/2

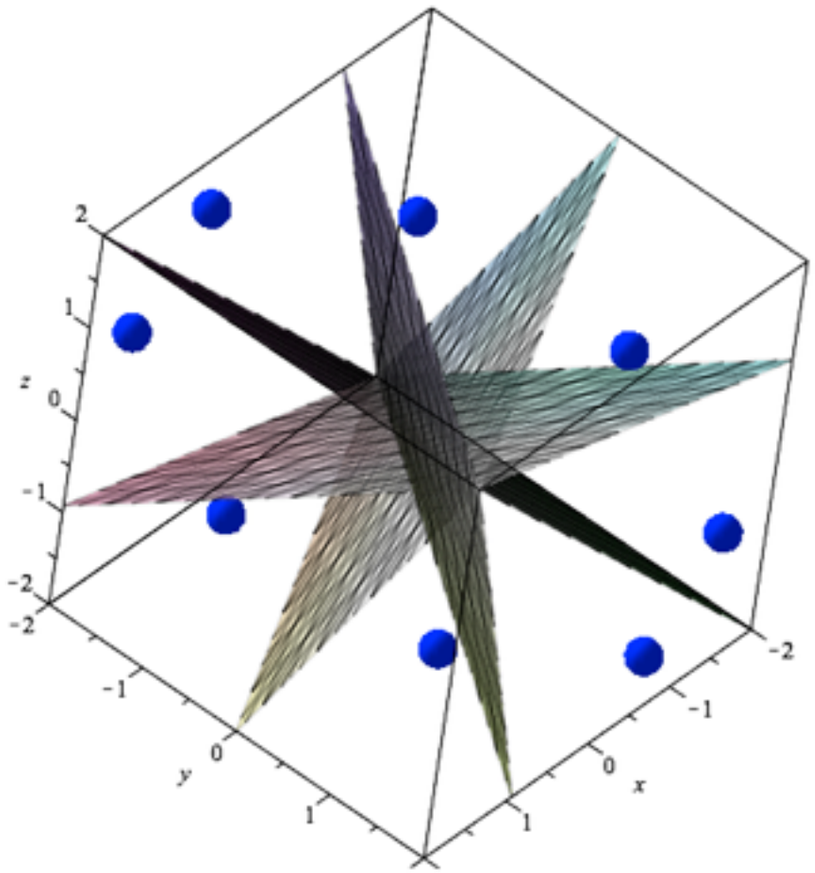


ISI-ratio = 1/1 = 1
Horiz. opening larger

ISI-ratio = (3/2)/(3/2)=1
Horiz. opening larger

ISI-Ratio can be Irrational

$$\mathrm{ISIR} = \sqrt{2} + 1$$



(3, 8, 4)-CC

Chordal Codes - Near Final Definition

A (*n, N, c, l*)-*Chordal Code* (CC) is a pair (C, Λ) where

- *C* is a subset of $[-1, 1]^n$ of size *N* (set of codewords on *n* wires)
- Λ is a subset of $(\mathbb{R}^n)^*$ of size *c* (set of comparators)

such that

- The coordinates of all codewords sum to zero
- The comparators vanish on (1,1,…,1).
- The L1-norm of the codewords is fixed (or has small variation)
- (Distinguishibility) $\forall c_1, c_2 \in C, c_1 \neq c_2 \exists \lambda \in \Lambda : \lambda(c_1)\lambda(c_2) < 0$
- (ISI-ratio) The ISI-ratio of all comparators w.r.t. *C* is ≤ *l*.

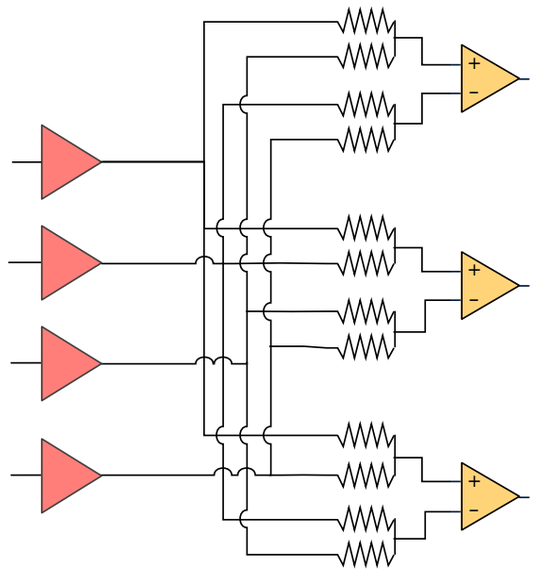
Given *n* and *N,* find minimum *l*, such that there exists a (*n, N, c, l*)-CC for some *c.*

ISI-Ratio = 1

- Matrices with orthogonal rows yield chordal codes of ISI-ratio 1.
- Only condition: sum of the columns is zero except at position 1
  - Enforces common mode resistance

ISI-Ratio 1: ENRZ Code

$$\frac{1}{3}\begin{pmatrix} 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \end{pmatrix}$$



ACTUAL IMPLEMENTATION
MAY BE DIFFERENT

$$\pm(1, -1/3, -1/3, -1/3)$$
$$\pm(-1/3, 1, -1/3, -1/3)$$
$$\pm(-1/3, -1/3, 1, -1/3)$$
$$\pm(-1/3, -1/3, -1/3, 1)$$

(Some) Bounds and Constructions

- ISI-ratio is always ≥ 1

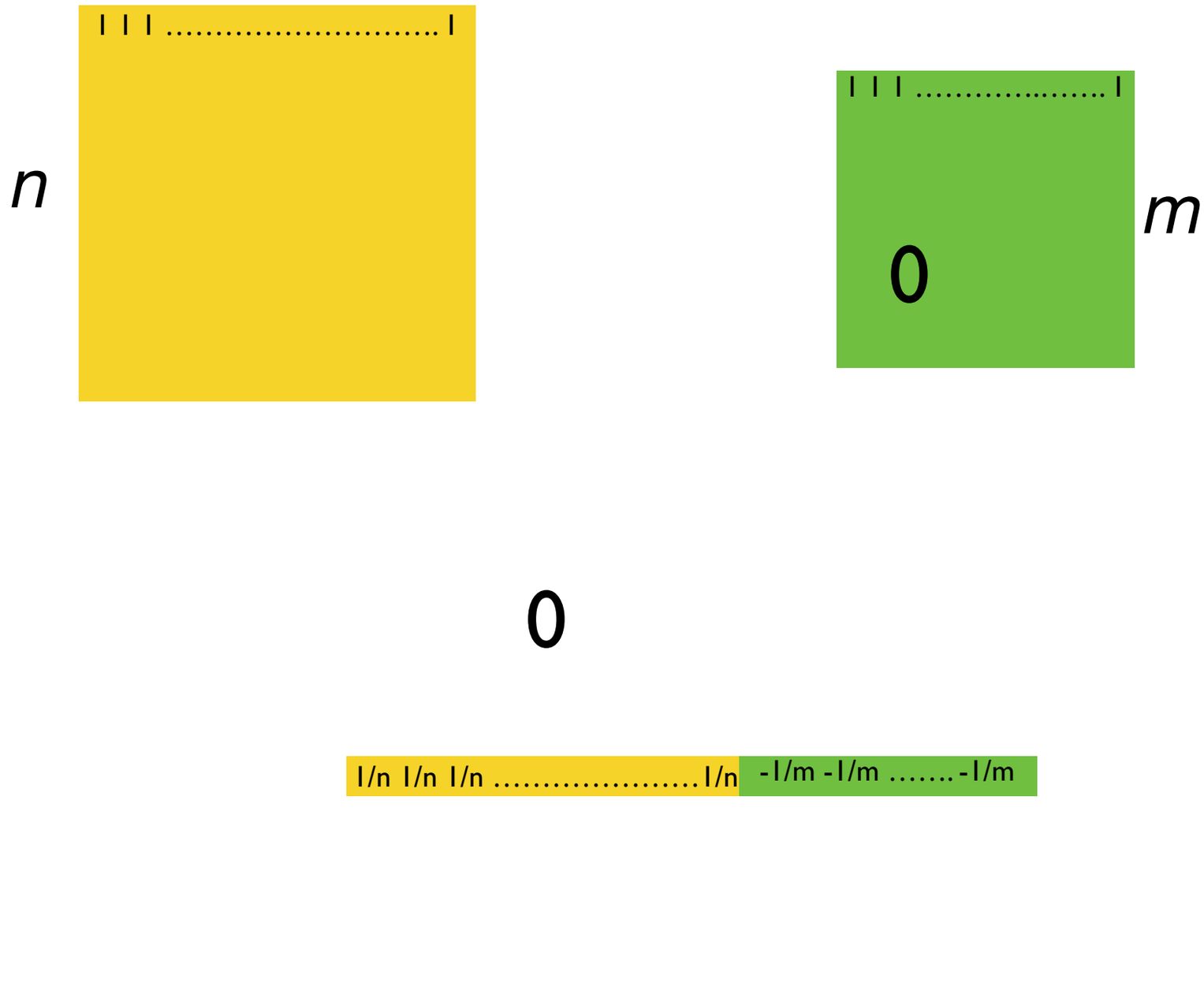
- For a (*n,N,c,l*)-CC we always have *c* ≥ *n.*

- For every *n* there is a (*n*, 2^{n-1}, *n*-1, 1)-CC.
  - (2, 2, 1, 1)-CC (differential signaling)
  - (3, 4, 2, 1)-CC (P3-code)
  - (4, 8, 3, 1)-CC (ENRZ code)
  - (6, 32, 5, 1)-CC (CNRZ-5 code)

- For large *n,* and integer *l,* we have a CC of ISI-ratio *l* and rate log(1+l).
  - Conjecture: The rate cannot be larger than log(1+*l*).

Proof: Haar Recursion

- Construct a chordal code of ISI-ratio 1 on *m*+*n* wires starting from CC's of ISI-ratio 1 on *m* and *n* wires



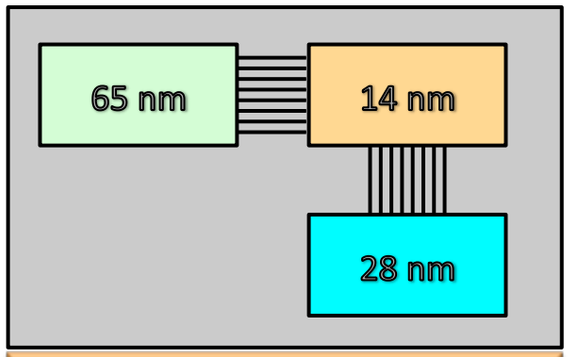
Proof: Haar Recursion

- Haar recursion yields appropriate matrices for any dimension *n.*
  - Start with dimensions 2 and 3 (NRZ and P3)
  - Use strong induction: assume that we have appropriate matrices for any dimension $< n$
- Apply Haar recursion to dimensions floor(n/2) and ceil(n/2), for example.

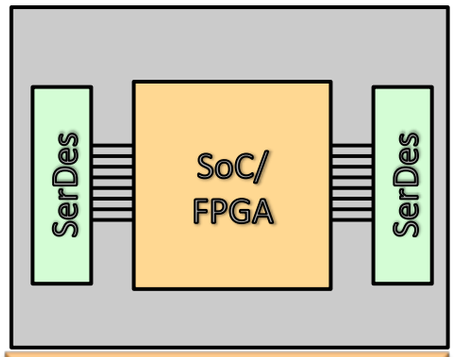
The Glasswing Chip

Application Space

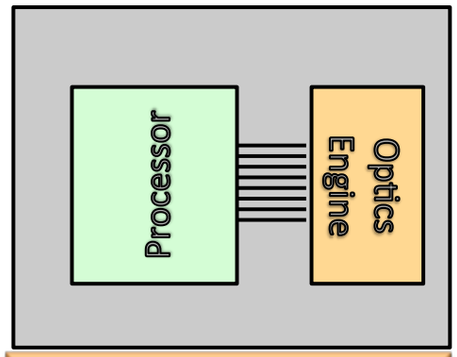
- Ultra-fast speed link connecting dies in a package
- Advantages include: yield improvement, faster time to market, lower development cost



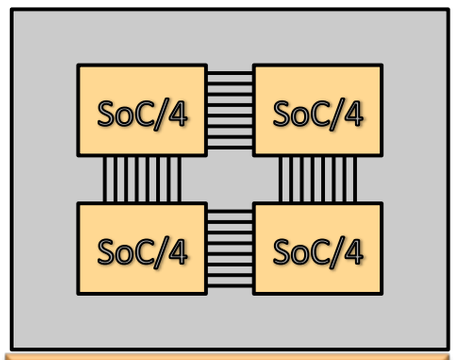
Packaging of dies with dissimilar semiconductor processes



Interface to off-chip SerDes



Interface to optics engine



Lego-like SoC design

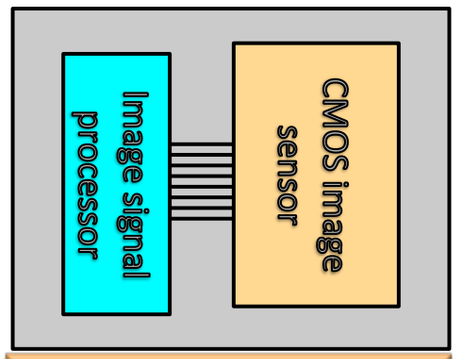
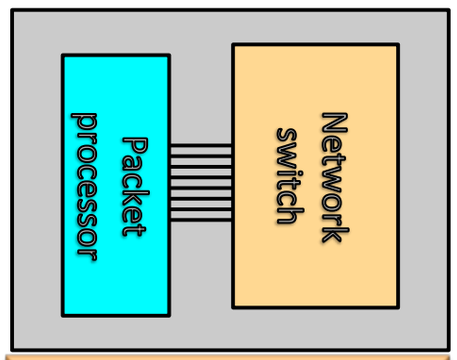


Image sensors



NS to PP links

Glasswing Code (CNRZ-5)

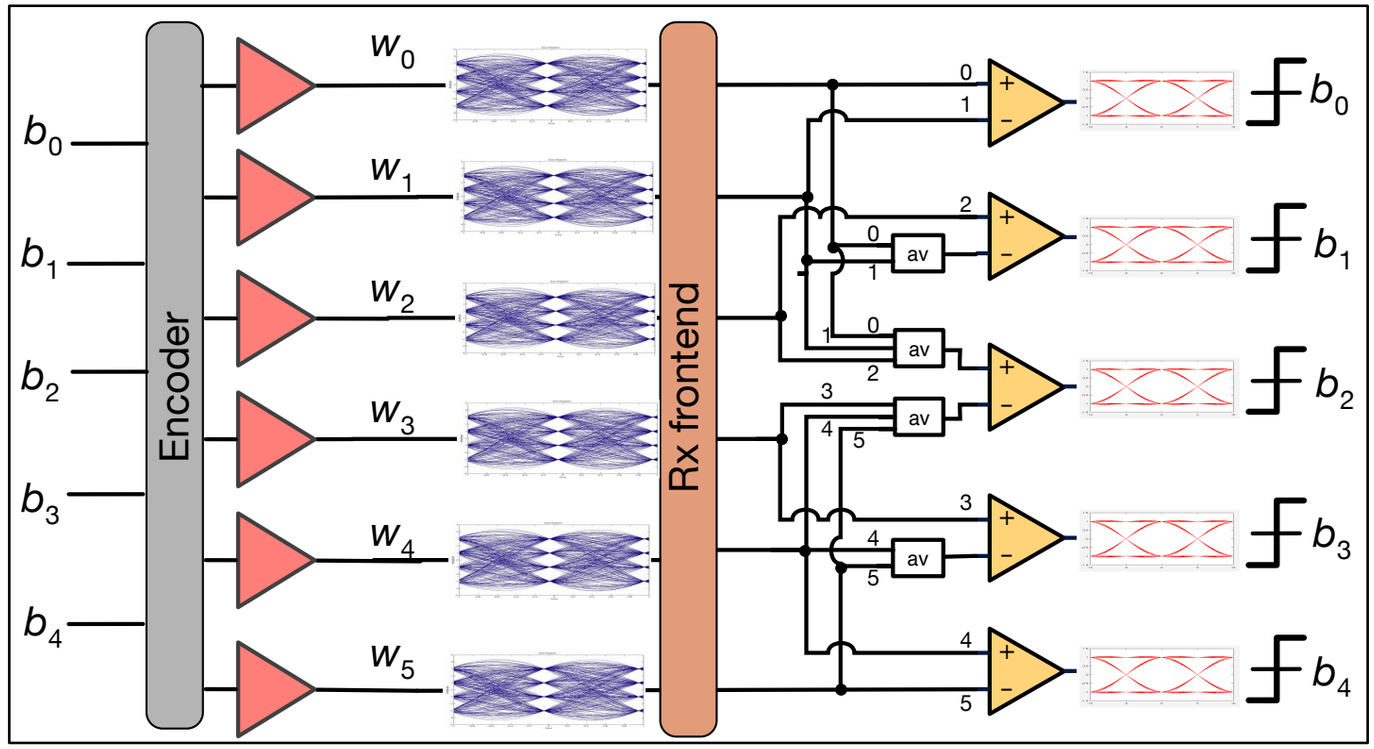
$$\frac{1}{3}(0,\pm1,\pm1,\pm1,\pm1,\pm1)\cdot\begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & 0 & -1 & 0 & 0 & 0 \\ 1 & -2 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & -2 & 1 \\ 0 & 0 & 0 & 1 & 0 & -1 \\ 1 & 1 & 1 & -1 & -1 & -1 \end{pmatrix}$$

- 5 bits on 6 wires, 1.66 times efficiency of differential signaling
- Obtained from Haar recursion applied to P3
- Excellent resilience to various types of noise

CNRZ-5 Codebook and Link

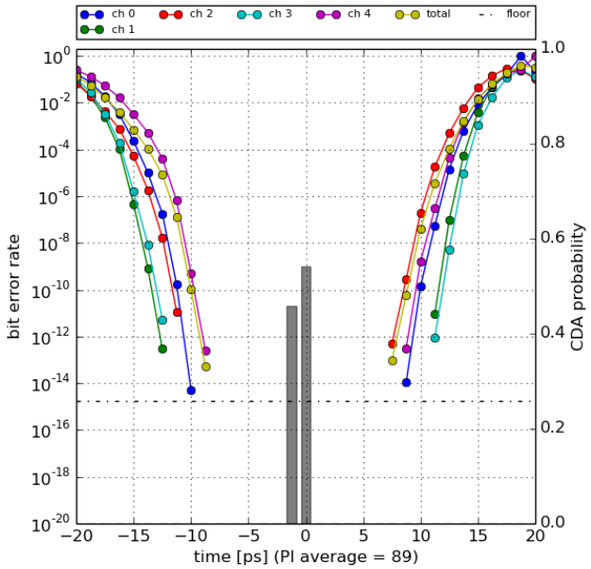
[1, 1/3, -1/3, -1, -1/3, 1/3]	[1/3, -1/3, -1, -1/3, 1/3, 1]
[1/3, 1, -1/3, -1, -1/3, 1/3]	[-1/3, 1/3, -1, -1/3, 1/3, 1]
[1/3, -1/3, 1, -1, -1/3, 1/3]	[-1/3, -1, 1/3, -1/3, 1/3, 1]
[-1/3, 1/3, 1, -1, -1/3, 1/3]	[-1, -1/3, 1/3, -1/3, 1/3, 1]
[1, 1/3, -1/3, -1, 1/3, -1/3]	[1/3, -1/3, -1, -1/3, 1, 1/3]
[1/3, 1, -1/3, -1, 1/3, -1/3]	[-1/3, 1/3, -1, -1/3, 1, 1/3]
[1/3, -1/3, 1, -1, 1/3, -1/3]	[-1/3, -1, 1/3, -1/3, 1, 1/3]
[-1/3, 1/3, 1, -1, 1/3, -1/3]	[-1, -1/3, 1/3, -1/3, 1, 1/3]
[1, 1/3, -1/3, 1/3, -1, -1/3]	[1/3, -1/3, -1, 1, -1/3, 1/3]
[1/3, 1, -1/3, 1/3, -1, -1/3]	[-1/3, 1/3, -1, 1, -1/3, 1/3]
[1/3, -1/3, 1, 1/3, -1, -1/3]	[-1/3, -1, 1/3, 1, -1/3, 1/3]
[-1/3, 1/3, 1, 1/3, -1, -1/3]	[-1, -1/3, 1/3, 1, -1/3, 1/3]
[1, 1/3, -1/3, 1/3, -1/3, -1]	[1/3, -1/3, -1, 1, 1/3, -1/3]
[1/3, 1, -1/3, 1/3, -1/3, -1]	[-1/3, 1/3, -1, 1, 1/3, -1/3]
[1/3, -1/3, 1, 1/3, -1/3, -1]	[-1/3, -1, 1/3, 1, 1/3, -1/3]
[-1/3, 1/3, 1, 1/3, -1/3, -1]	[-1, -1/3, 1/3, 1, 1/3, -1/3]

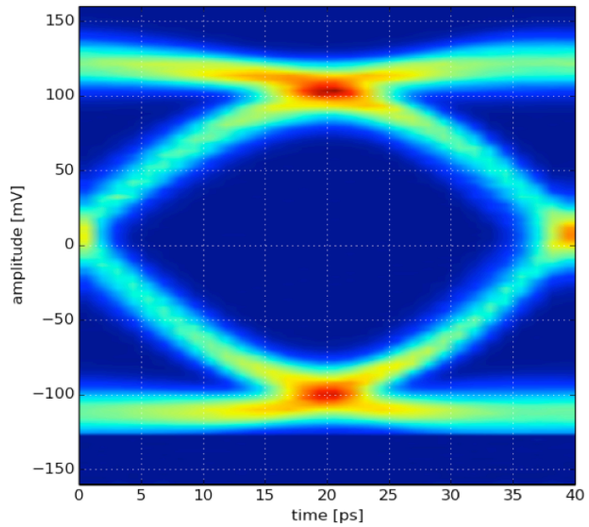
CNRZ-5 Codebook

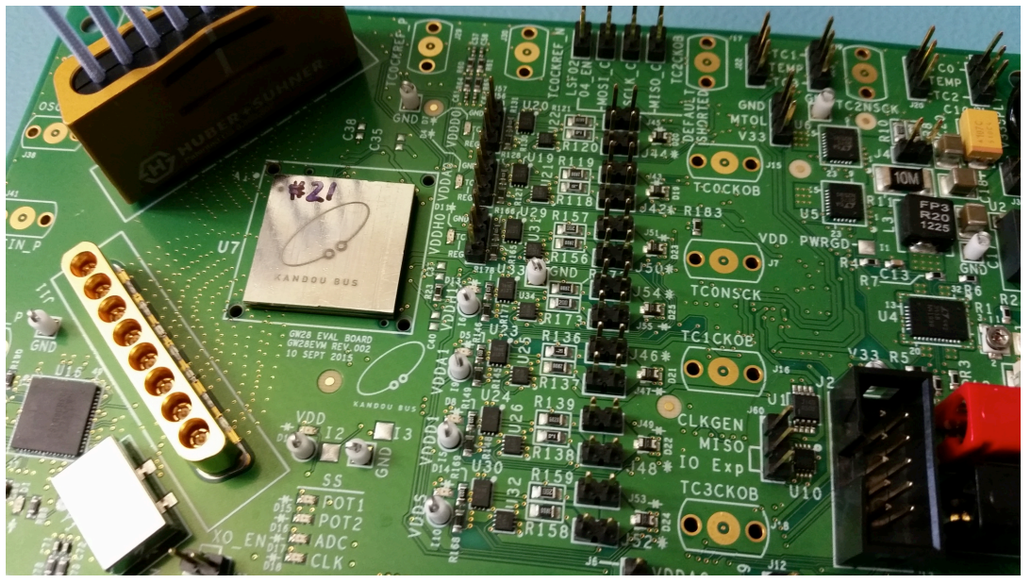


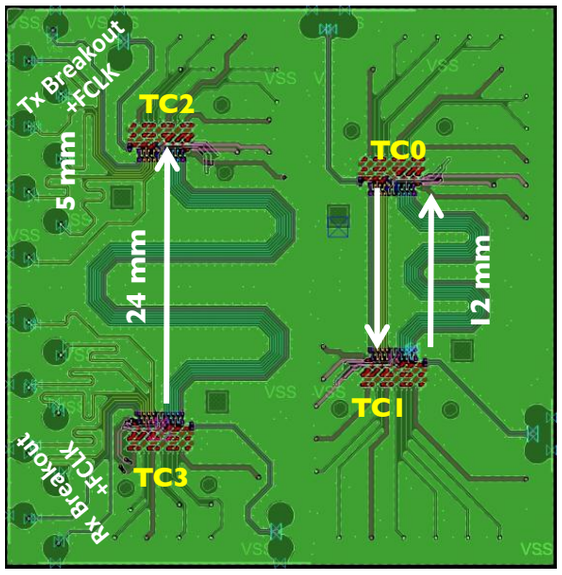
Glasswing

- Fully characterized.
- Power consumption is ~30% of comparable products
- Highest speed for in-package SerDes (more than 20Gbps/wire)

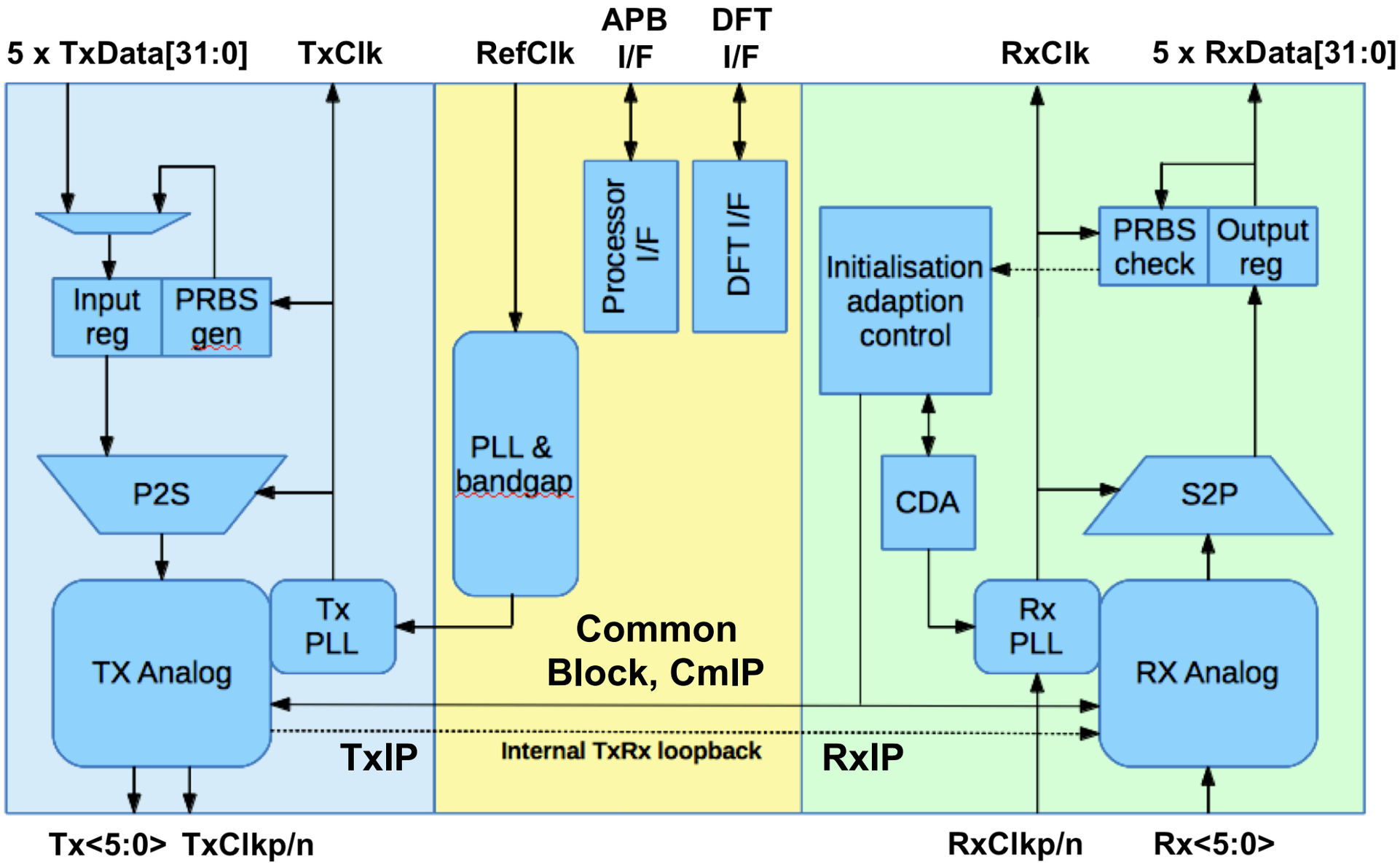








Glasswing Chip: Macro Architecture



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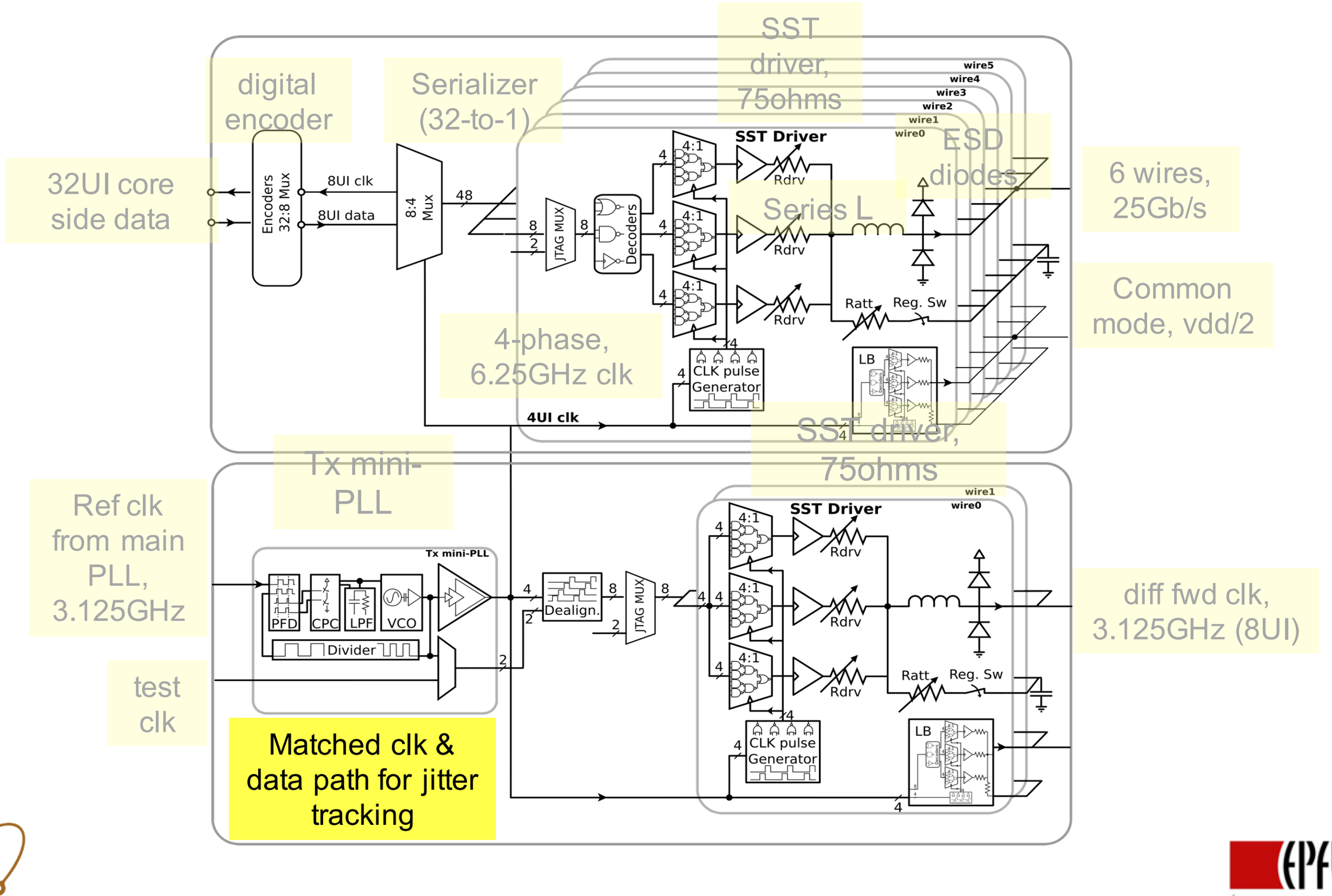
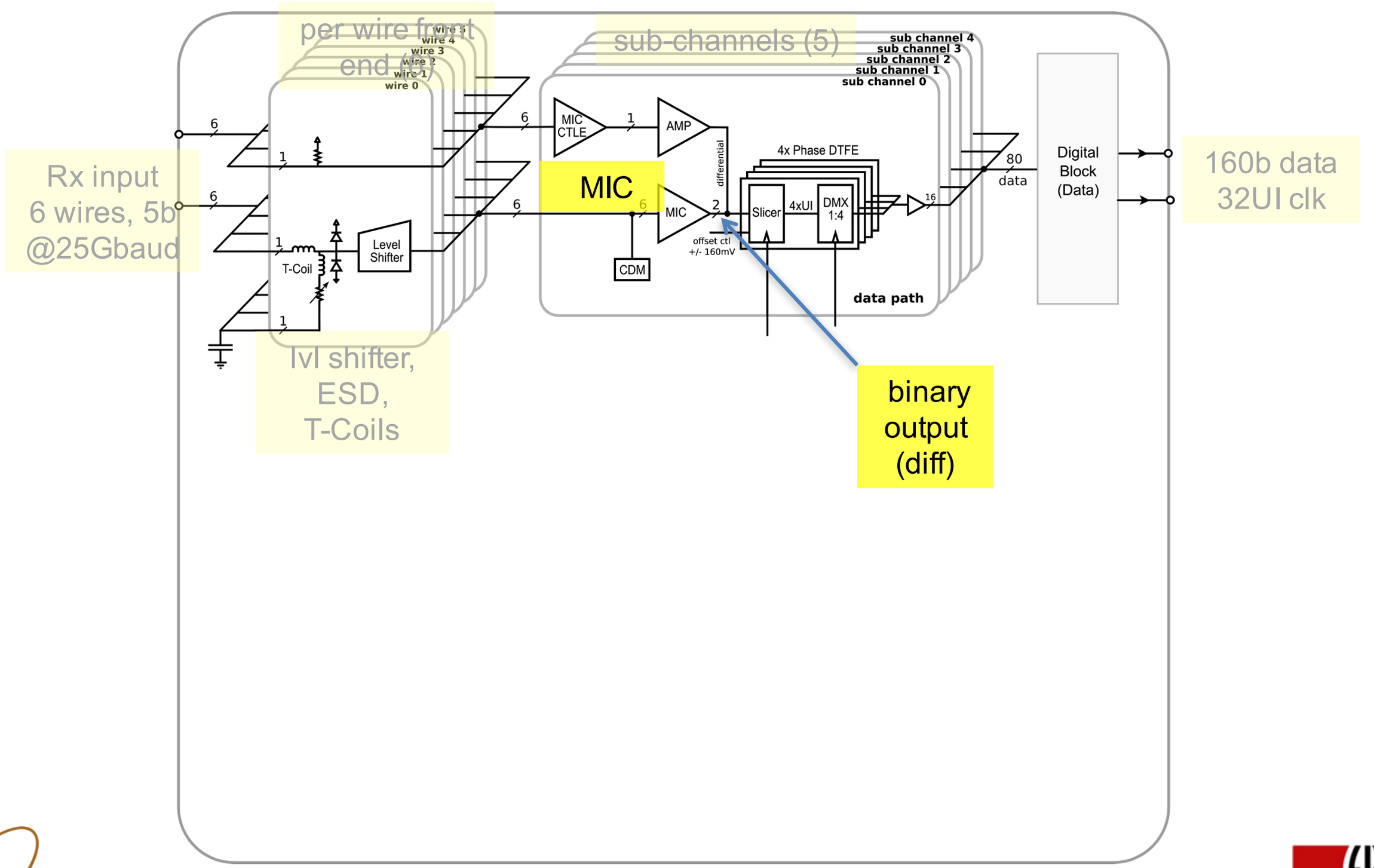
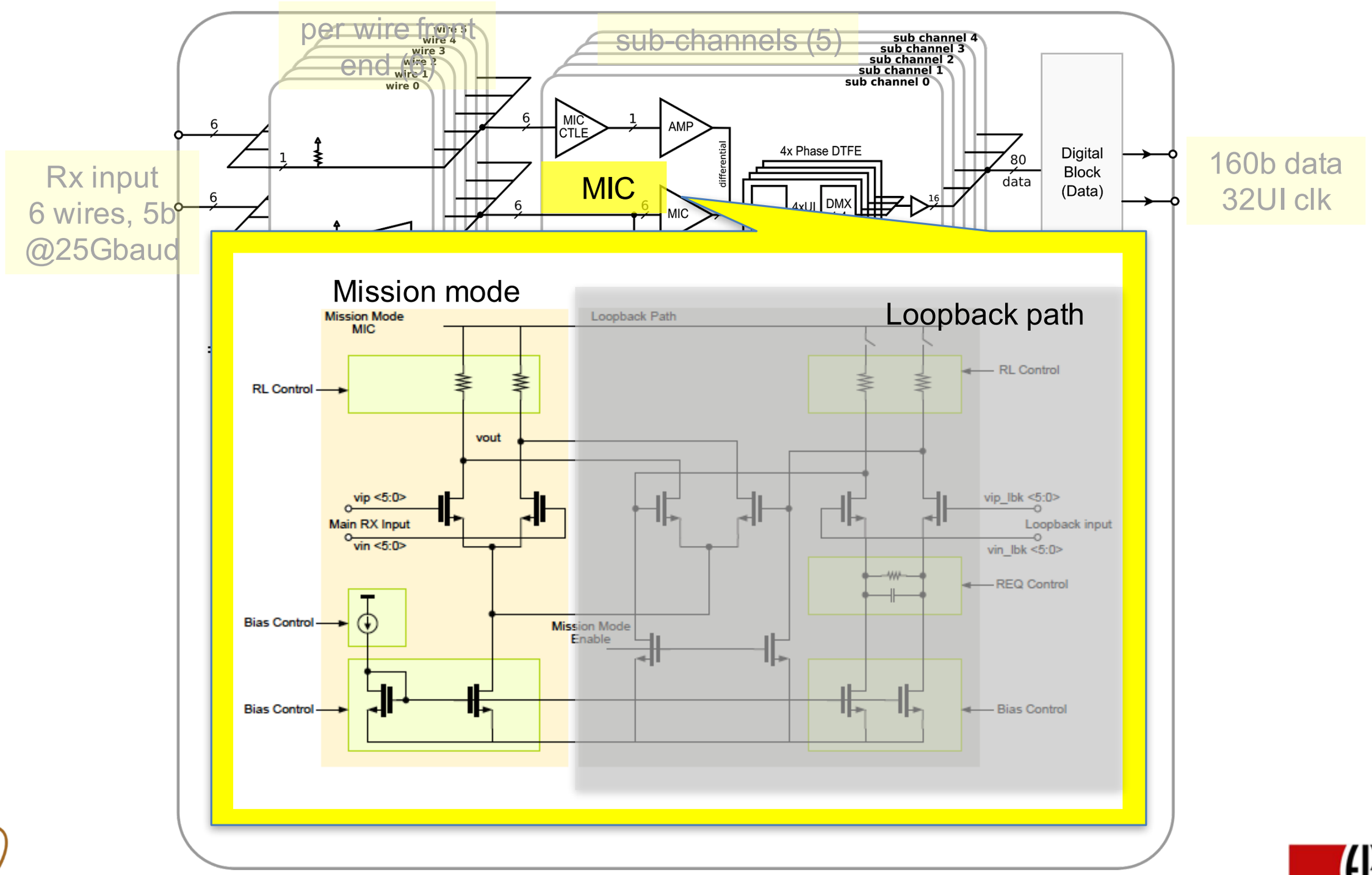
Transmitter



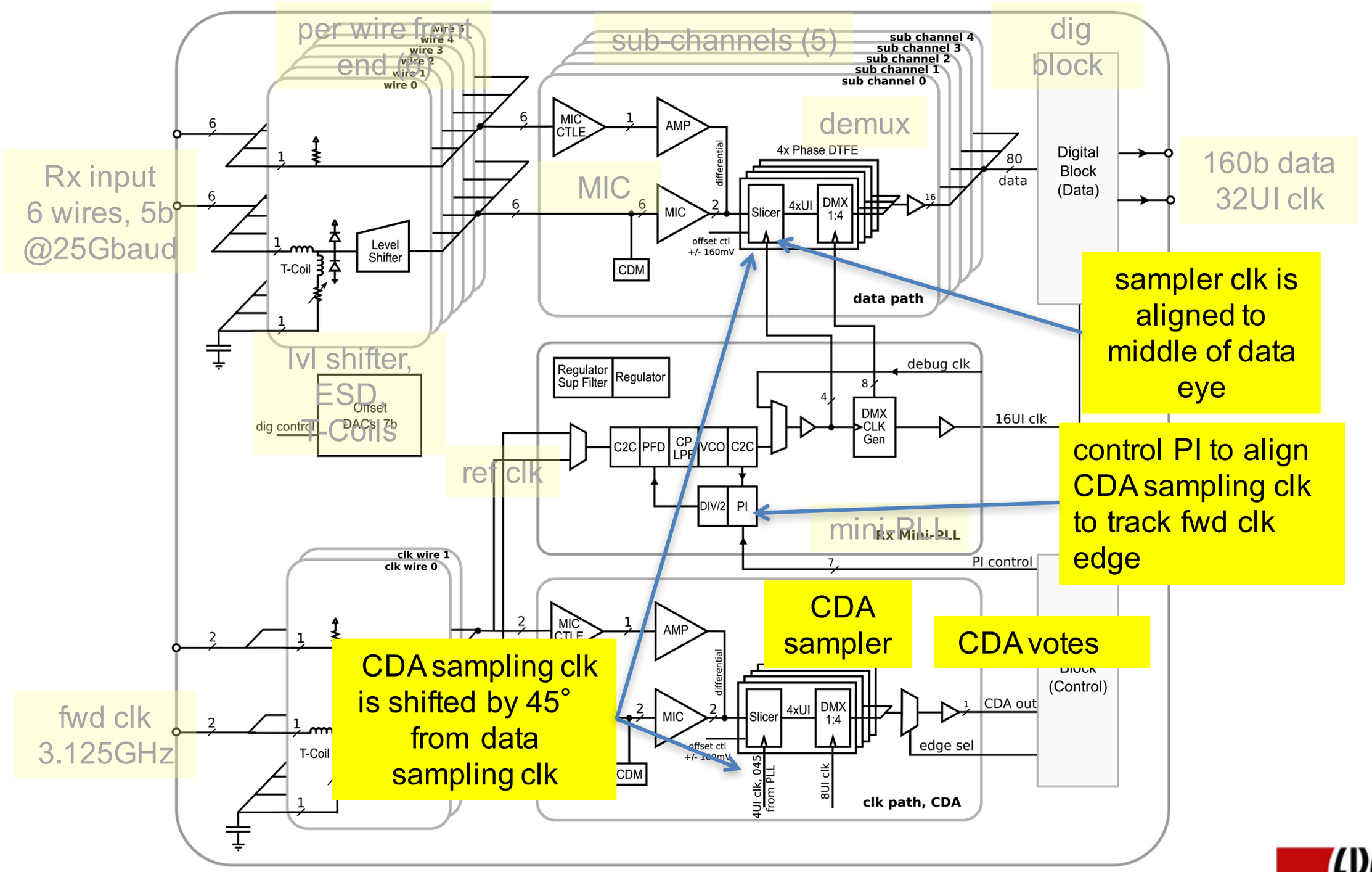
Receiver


per wire front end (6)
wire 5
wire 4
wire 3
wire 2
wire 1
wire 0
sub-channels (5)
sub channel 4
sub channel 3
sub channel 2
sub channel 1
sub channel 0
Rx input
6 wires, 5b
@25Gbaud
6
1
T-Coil
Level Shifter
lvl shifter, ESD, T-Coils
MIC CTLE
AMP
MIC
differential
4x Phase DTFE
Slicer
4xUI
DMX 1:4
16
80
data
Digital Block (Data)
160b data
32UI clk
CDM
offset ctl
+/- 160mV
data path
binary output (diff)

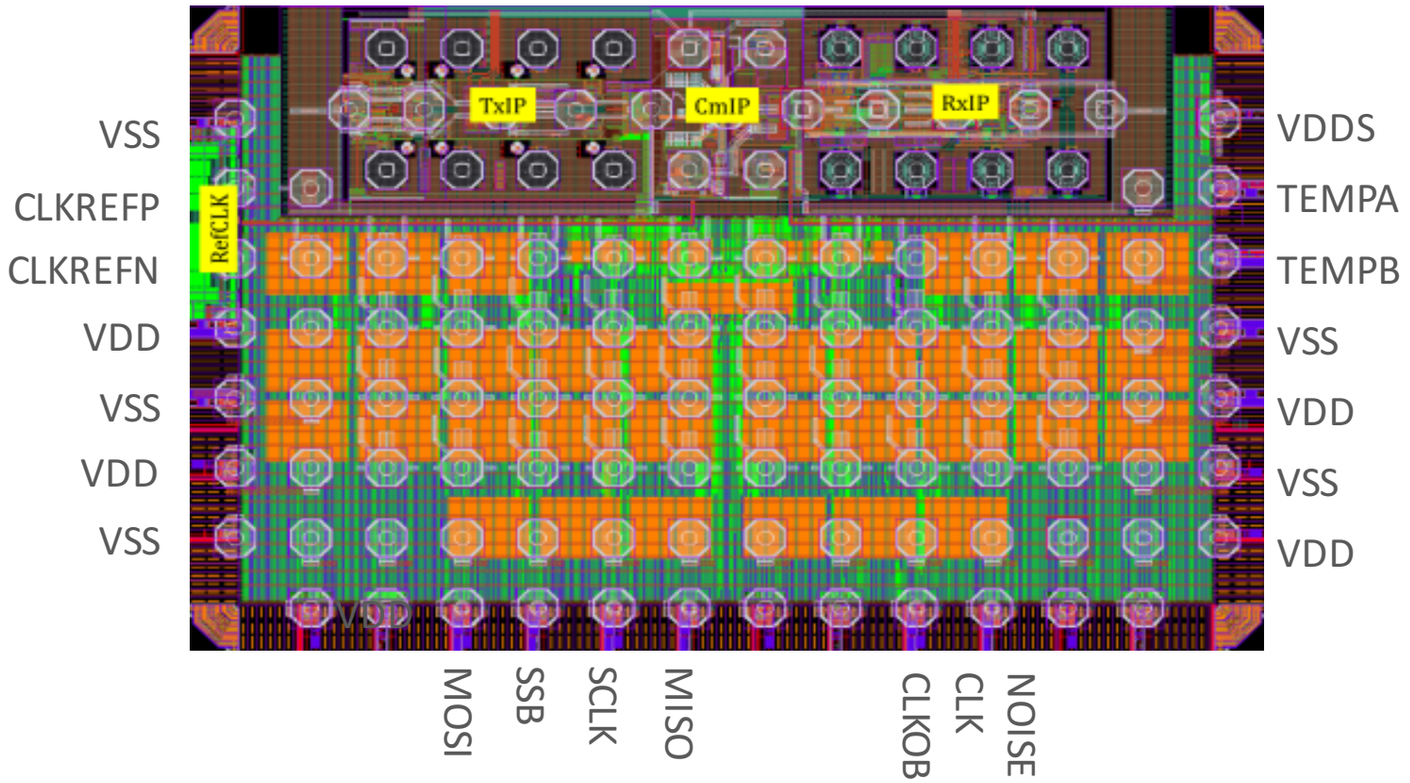
Multi-Input Comparators

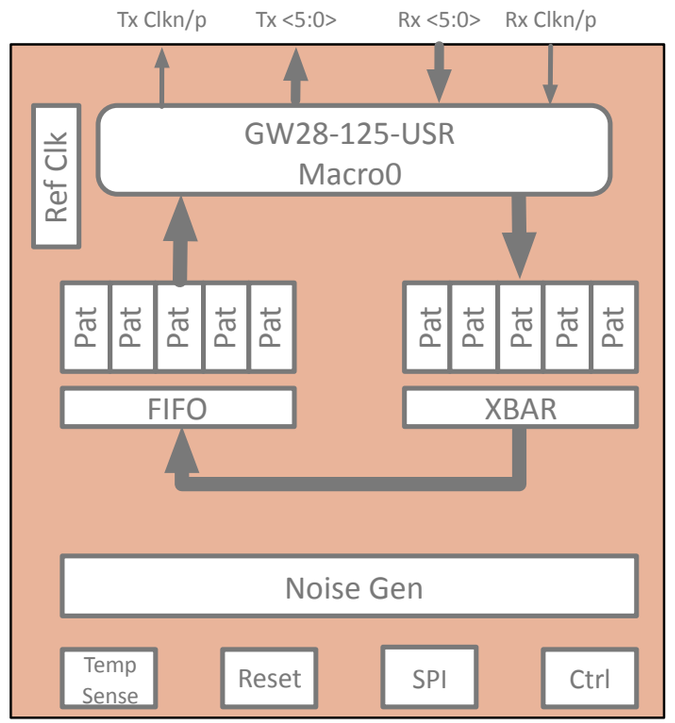


Receiver


per wire front end (6)
wire 5
wire 4
wire 3
wire 2
wire 1
wire 0
sub-channels (5)
sub channel 4
sub channel 3
sub channel 2
sub channel 1
sub channel 0
dig block
demux
MIC
Rx input
6 wires, 5b
@25Gbaud
MIC CTLE
AMP
differential
4x Phase DTFE
Slicer
4xUI
DMX 1:4
80
data
Digital Block (Data)
160b data
32UI clk
offset ctl
+/- 160mV
CDM
T-Coil
Level Shifter
data path
sampler clk is aligned to middle of data eye
lvl shifter, ESD, T-Coils
Offset DACs 7b
dig control
Regulator Sup Filter
Regulator
debug clk
C2C
PFD
CP LPF
VCO
C2C
DMX CLK Gen
16UI clk
ref clk
DIV/2
PI
mini-PLL
Rx Mini-PLL
control PI to align CDA sampling clk to track fwd clk edge
PI control
clk wire 1
clk wire 0
CDA sampler
CDA votes
CDA sampling clk is shifted by 45° from data sampling clk
fwd clk
3.125GHz
CDA out
edge sel
4UI clk, 045 from PLL
8UI clk
clk path, CDA

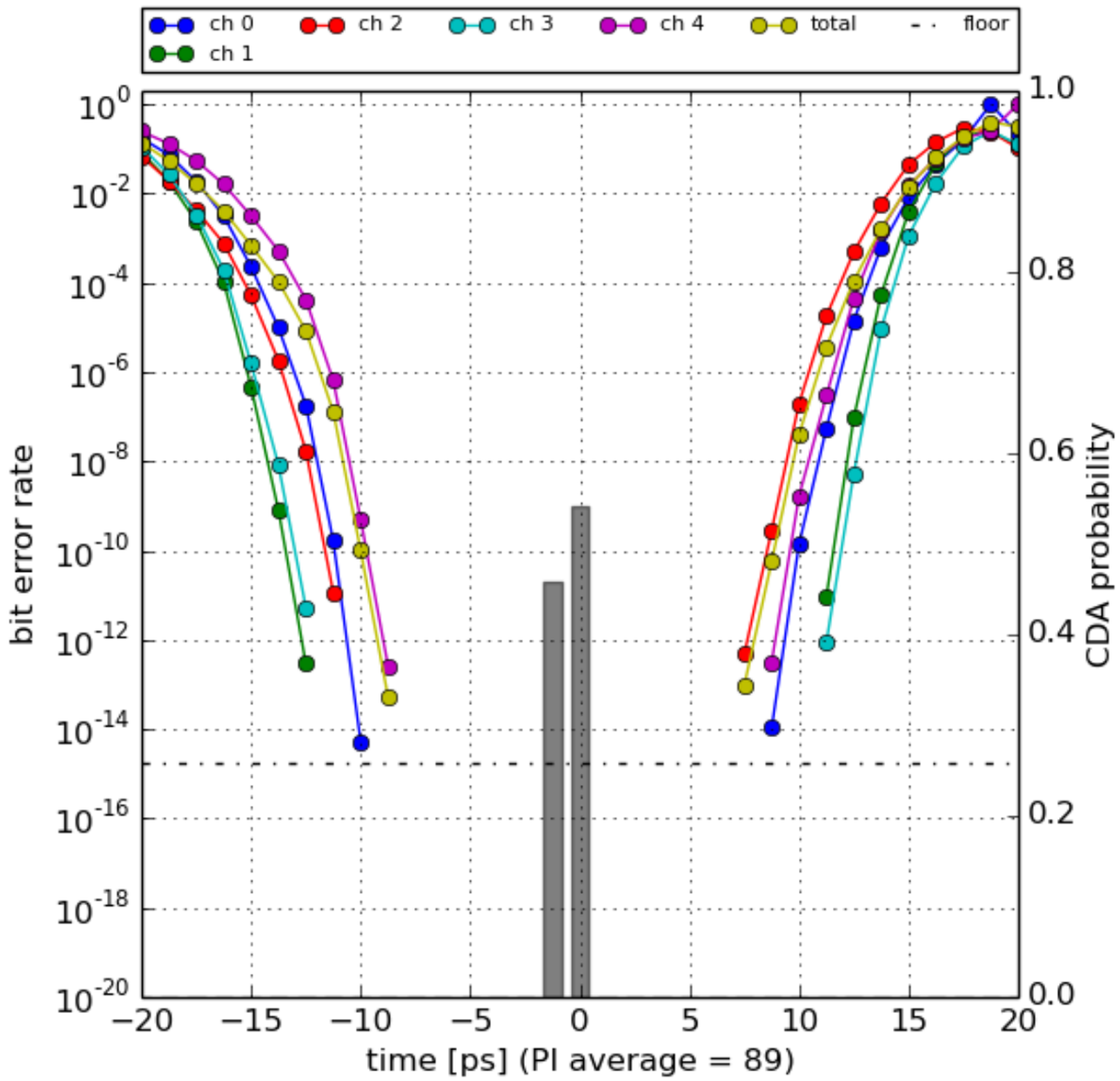
Test Chip

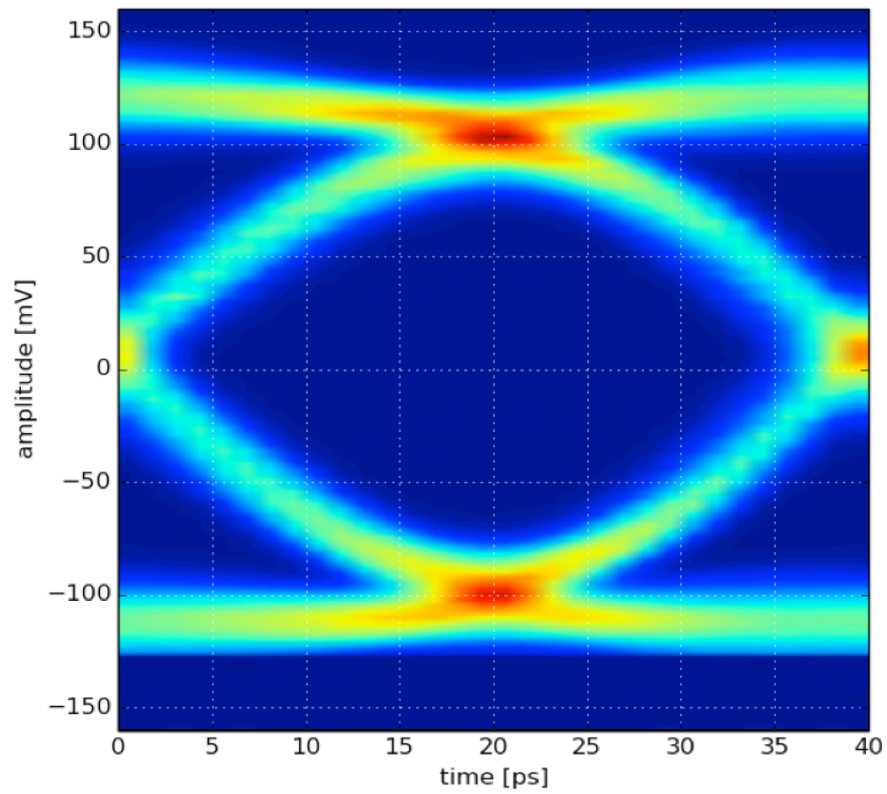




- Architecture:
  - One instance of CNRZ-5 IP (Tx + Rx)
  - One common block
  - 62.5 Gb/s and 125 Gb/s over six wires
- Die size (actual without scribe) 2138.4µm x 1386.9µm (2.96sqmm)

Results


ch 0
ch 1
ch 2
ch 3
ch 4
total
floor
bit error rate
CDA probability
time [ps] (PI average = 89)

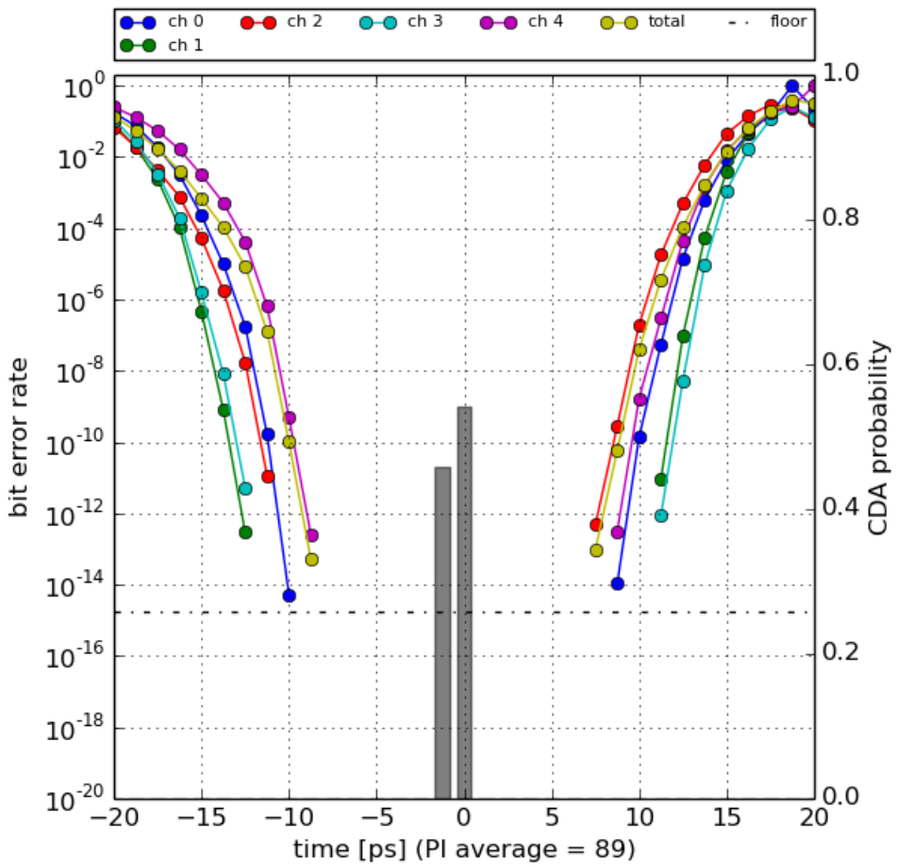

amplitude [mV]
time [ps]

Measured Power at 125 Gbps

		V	mA	mW		
CMIP	VDDA	0.925	2.253	**2.084**	*1.77%*	*8.48%*
	VDDH	1.400	5.616	**7.862**	*6.69%*	
	VDDD	0.800	0.032	**0.026**	*0.02%*	
TXIP	VDDA	0.925	54.927	**50.807**	*43.20%*	*54.17%*
	VDDH	1.400	3.996	**5.594**	*4.76%*	
	VDDD	0.800	9.125	**7.300**	*6.21%*	
RXIP	VDDA	0.925	31.152	**28.816**	*24.50%*	*37.35%*
	VDDH	1.400	8.177	**11.448**	*9.73%*	
	VDDD	0.800	4.584	**3.667**	*3.12%*	
			P_{total} [mW]	**117.605**		
			Rate [Gb/s]	125		
			E_{bit} [pJ/b]	**0.941**		

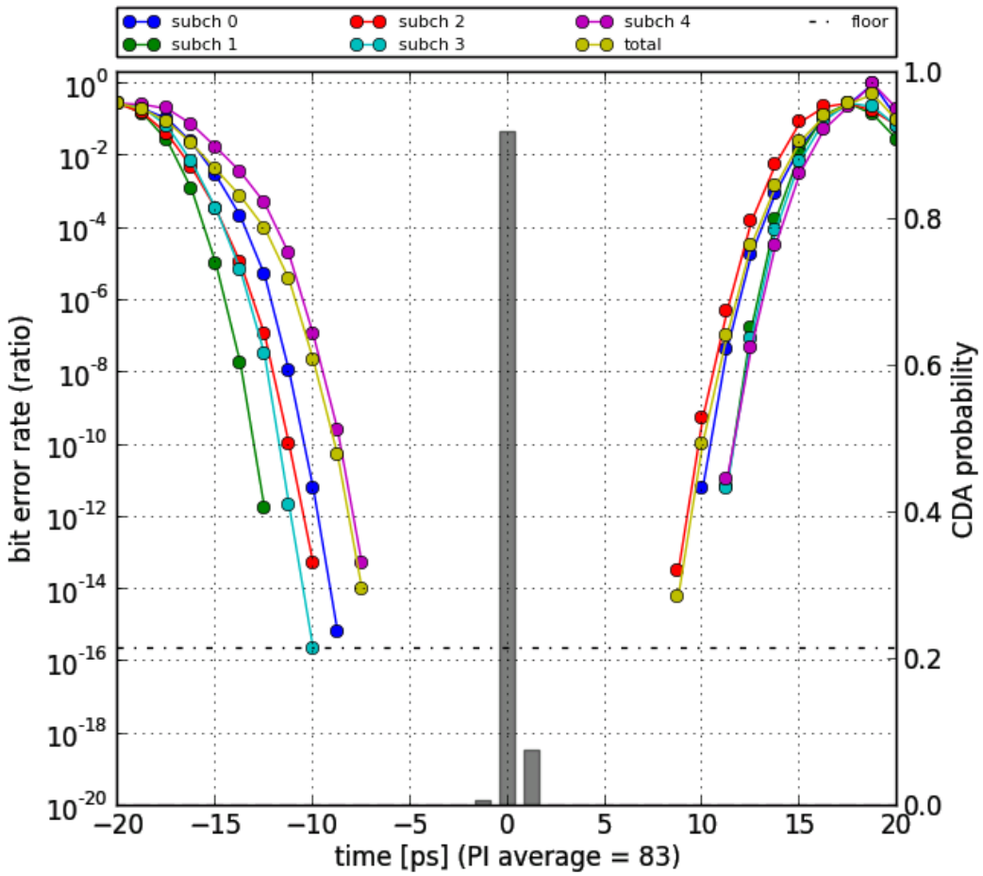
Results

0.94 pJ/b



Vdda = 0.925V
Vddd = 0.8V
Vddh = 1.4V

1.04 pJ/b



Vdda = 1V
Vddd = 1V
Vddh = 1.5V

Conclusions

- Chip-to-chip communication is one of the areas of communication where information theory has not yet been used
- Normal operating rules of information theory do not hold in this domain, since most of the power is spent in processing
- Chordal codes are a first step towards a coding theory with built-in resilience to noise and built-in decoding procedure
- We expect chordal codes to be in products in 2018